Datasheet

APM32F103x4x6x8xb

ARM® Cortex®-M3 based 32-bit MCU

Version: 05/2019

1 Features

- **System Architecture**
  - ARM® 32-bit Cortex®-M3 core
  - 96MHz maximum frequency, 1.5DMIPS/MHz performance at 0 wait state memory access
- **Power, Clock and Reset**
  - 2.0 to 3.6 V application supply
  - 4MHz~16MHz external crystal oscillator
  - 32KHz RTC oscillator for RTC with calibration
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - POR, PDR, and programmable voltage detector (PVD)
- **Memories**
  - 128 Kbytes of Flash memory
  - 20 Kbytes of SRAM
- **Low-power**
  - Sleep, Stop and Standby modes
  - Support battery, RTC and backup registers
- **FPU**
  - Independent FPU module supports floating point operations
- **2 x 12-bit ADCs and Temperature Sensor**
  - Conversion time: 1 μs (up to 16 channels)
  - Conversion range: 0~VDDA
  - Double-sample and hold capability
  - On-chip temperature sensor
- **I / O**
  - 80/51/37/26 I/Os (depend on models and packages)
  - All mappable on 16 external interrupt vectors
  - Almost all 5 V-tolerant
- **DMA**
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs,I2Cs and USARTs
- **Timers and PWM**
  - Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 16-bit, motor control PWM timer with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - 1 SysTick timer 24-bit downcounter
- **Communication Interfaces**
  - 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - 2 x I^2C interfaces (SMBus/PMBus)
  - 2 SPIs (18 Mbit/s)
  - 1 QSPI interface (Dual-Flash/ Quad-SPI)
  - 1 USB 2.0 full-speed interface
  - 1 CAN 2.0B interface (USB and CAN can work independently at the same time)
- **CRC Unit**
  - 1 CRC calculation unit, 96-bit unique ID

- **Debug Mode**
  - Serial wire debug (SWD) & JTAG interfaces
- **Chip Package**
  - LQFP100/LQFP64/LQFP48/QFN36
- **Field of Application**
  - Medical equipment, PC peripherals, industrial control, smart meters, household appliances

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1.1 Overview

The APM32F103x4x6x8xB/APM32E103xB series of chips is a 32-bit microprocessor based on the ARM® Cortex®-M3 core with a maximum operating frequency of 96MHz. Built-in AHB high-performance bus, combined with high-speed memory and DMA for fast data processing and storage. The built-in APB advanced peripheral bus expands the rich peripherals and enhanced I/O, ensuring fast connection and control flexibility. The chip is equipped with a powerful FPU floating-point arithmetic processing unit that supports single-precision data processing instructions and data types.

Built-in up to 128K bytes of flash memory and 20K bytes of SRAM memory, all models include two 12-bit ADCs, three general-purpose 16-bit timers, one advanced control timer and one temperature sensor, as well as standard and advanced communication interfaces: 2 I^2Cinterfaces, 2 SPI interfaces, 1 QSPI interface, 3 USART interfaces, 1 USB 2.0 FS interface and 1 CAN 2.0B interface. USB and CAN can work independently at the same time.

Operating voltage is 2.0V ~ 3.6V, there are two types of operating temperature range for choosing: -40°C to +85°C and -40°C to +105°C. Available in four different package forms of LQFP100/LQFP64/LQFP48/QFN36, with different peripherals and I/O configurations.

1.2 Model Configuration

Table 1 APM32F103x4x6x8xB/APM32E103xB Product Features and Peripheral Counts

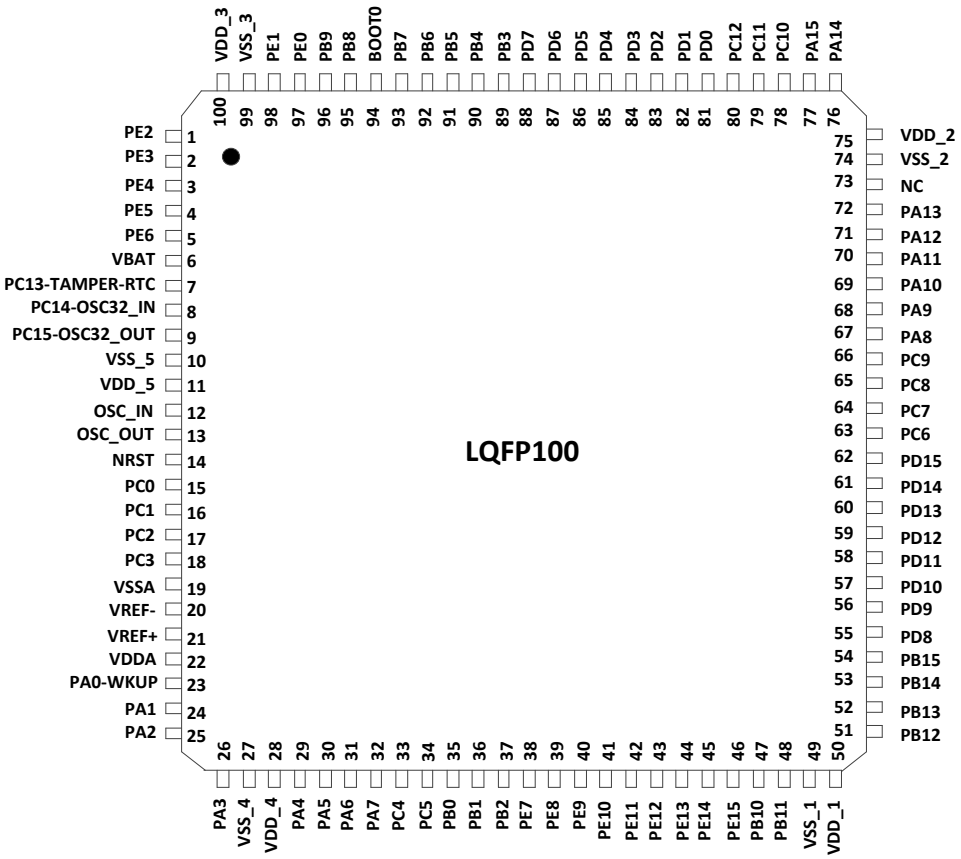
Part number		APM32F103xx														APM32E103xx		
		T4	T6	T8	TB	C4	C6	C8	CB	R4	R6	R8	RB	V8	VB	CB	RB	VB
Packages		QFN36				LQFP48				LQFP 64				LQFP 100		LQFP 48	LQFP 64	LQFP 100
Flash (Kbytes)		16	32	64	128	16	32	64	128	16	32	64	128	64	128	128	128	128
SRAM (Kbytes)		6	10	20	20	6	10	20	20	4	10	20	20	20	20	20	20	20
Timers	General (16-bit)	2	2	3	3	2	2	3	3	2	2	3	3	3	3	3	3	3
	Advanced (16-bit)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Communication	SPI	1	1	1	1	1	1	2	2	1	1	2	2	2	2	2	2	2
	QSPI	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	I²C	1	1	1	1	1	1	2	2	1	1	2	2	2	2	2	2	2
	USART	2	2	2	2	2	2	3	3	2	2	3	3	3	3	3	3	3
	CAN2.0B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USB2.0 FS	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12 bit ADC	Unit	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	Channel	10	10	10	10	10	10	10	10	16	16	16	16	16	16	10	16	16
GPIOs		26	26	26	26	37	37	37	37	51	51	51	51	80	80	37	51	80
CPU@Max. frequency		M3@72MHz														M3@96MHz		
FPU		-														Support FPU unit		
Operating voltage		2.0 V~ 3.6 V																

2 3-Pin Features

2.1 Pinouts and Pin Description

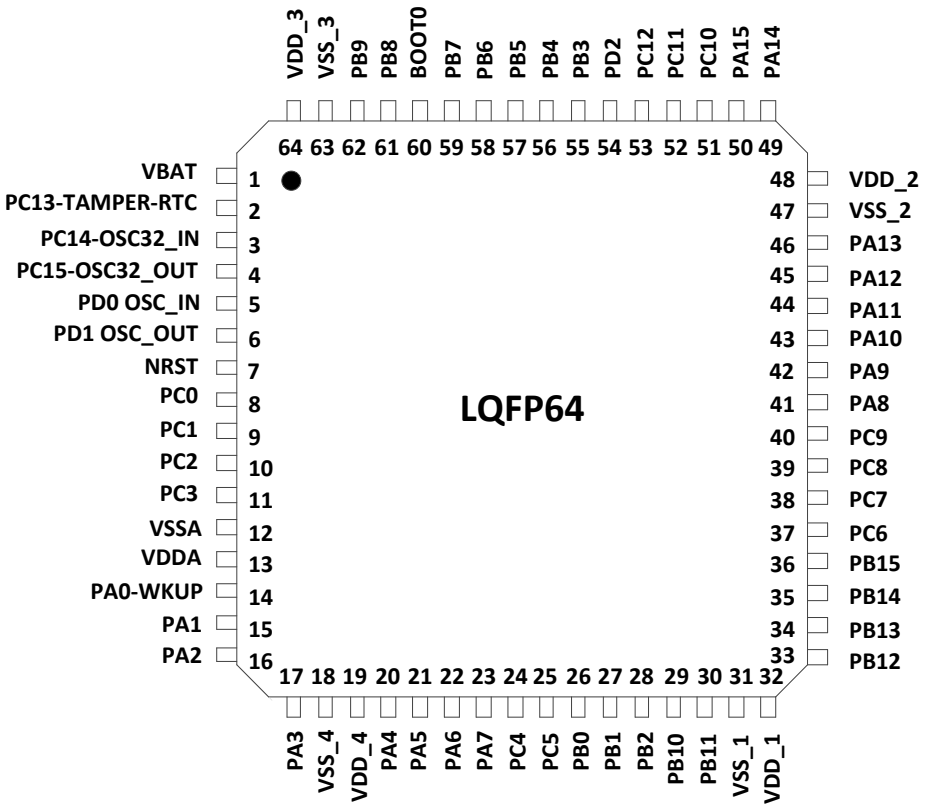
2.1.1 APM32F103x4x6x8xB/APM32E103VB Series LQFP100

Figure 1 LQFP100 Pinout



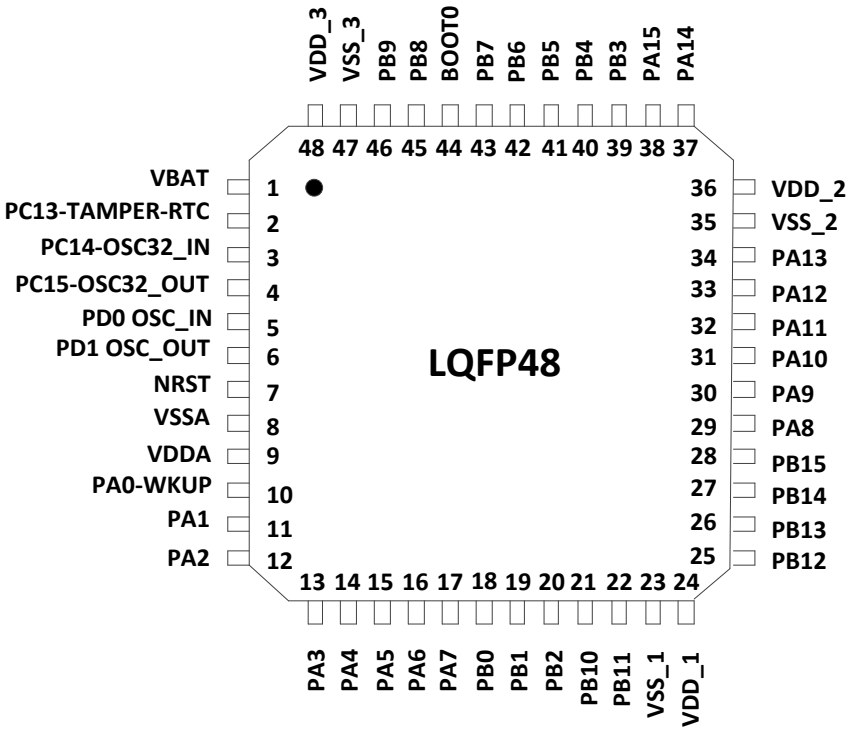
2.1.2 APM32F103x4x6x8xB/APM32E103RB Series LQFP64

Figure 2 LQFP64 Pinout



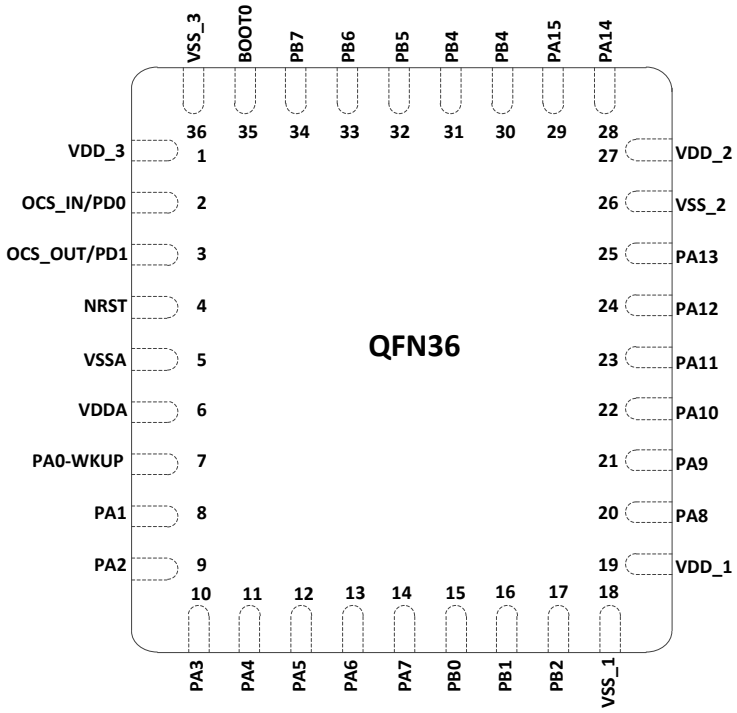
2.1.3 APM32F103x4x6x8xB/APM32E103CB Series LQFP48

Figure 3 LQFP48 Pinout



2.1.4 APM32F103 x4x6x8xB Series QFN36

Figure 4 QFN36 Pinout



2.2 Pin Description

Table 2 APM32F103x4x6x8xB/APM32E103xB Pin Definitions

Pin Name	Pins				Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP48	LQFP64	LQFP100	QFN36			(after reset)	Default	Remap
PE2	-	-	1	-	I/O	FT	PE2	TRACECK	-
PE3	-	-	2	-	I/O	FT	PE3	TRACED0	-
PE4	-	-	3	-	I/O	FT	PE4	TRACED1	-
PE5	-	-	4	-	I/O	FT	PE5	TRACED2	-
PE6	-	-	5	-	I/O	FT	PE6	TRACED3	-
V_{BAT}	1	1	6	-	S	-	V_{BAT}	-	-
PC13-TAMPER-RTC(4)	2	2	7	-	I/O	-	PC13(5)	TAMPER-RTC	-
PC14-OSC32_IN(4)	3	3	8	-	I/O	-	PC14(5)	OSC32_IN	-
PC15-OSC32_OUT(4)	4	4	9	-	I/O	-	PC15(5)	OSC32_OUT	-
V_{SS}_5	-	-	10	-	S	-	V_{SS}_5	-	-
V_{DD}_5	-	-	11	-	S	-	V_{DD}_5	-	-
OSC_IN	5	5	12	2	I	-	OSC_IN	-	PD0(7)
OSC_OUT	6	6	13	3	O	-	OSC_OUT	-	PD1(7)
NRST	7	7	14	4	I/O	-	NRST	-	-
PC0	-	8	15	-	I/O	-	PC0	ADC12_IN10	-
PC1	-	9	16	-	I/O	-	PC1	ADC12_IN11	-
PC2	-	10	17	-	I/O	-	PC2	ADC12_IN12	-
PC3	-	11	18	-	I/O	-	PC3	ADC12_IN13	-
V_{SSA}	8	12	19	5	S	-	V_{SSA}	-	-
V_{REF-}	-	-	20	-	S	-	V_{REF-}	-	-
V_{REF+}	-	-	21	-	S	-	V_{REF+}	-	-
V_{DDA}	9	13	22	6	S	-	V_{DDA}	-	-

PA0-WKUP	10	14	23	7	I/O	-	PA0	WKUP/USART2_CTS(6)/ ADC12_IN0/TIM2_CH1_ETR(6)	-
PA1	11	15	24	8	I/O	-	PA1	USART2_RTS(6)/ADC12_IN1/ TIM2_CH2(6)	-
PA2	12	16	25	9	I/O	-	PA2	USART2_TX(6)/ADC12_IN2/ TIM2_CH3(6)	-
PA3	13	17	26	10	I/O	-	PA3	USART2_RX(6)/ ADC12_IN3/ TIM2_CH4(6)	-
V_{SS}_4	-	18	27	-	S	-	V_{SS}_4	-	-
V_{DD}_4	-	19	28	-	S	-	V_{DD}_4	-	-
PA4	14	20	29	11	I/O	-	PA4	SPI1_NSS(6)/USART2_CK(6)/ ADC12_IN4	-
PA5	15	21	30	12	I/O	-	PA5	SPI1_SCK(6)/ADC12_IN5	-
PA6	16	22	31	13	I/O		PA6	SPI1_MISO(7)/ ADC12_IN6/TIM3_CH1(7)	TIM1_BKIN
PA7	17	23	32	14	I/O		PA7	SPI1_MOSI(7)/ ADC12_IN7/TIM3_CH2(7)	TIM1_CH1N
PC4	-	24	33	-	I/O	-	PC4	ADC12_IN14	-
PC5	-	25	34	-	I/O	-	PC5	ADC12_IN15	-
PB0	18	26	35	15	I/O	-	PB0	ADC12_IN8/TIM3_CH3(6)	TIM1_CH2N
PB1	19	27	36	16	I/O	-	PB1	ADC12_IN9/TIM3_CH4(6)	TIM1_CH3N
PB2	20	28	37	17	I/O	FT	PB2/BOOT1	-	-
PE7	-	-	38	-	I/O	FT	PE7	-	TIM1_ETR
PE8	-	-	39	-	I/O	FT	PE8	-	TIM1_CH1N
PE9	-	-	40	-	I/O	FT	PE9	-	TIM1_CH1
PE10	-	-	41	-	I/O	FT	PE10	-	TIM1_CH2N
PE11	-	-	42	-	I/O	FT	PE11	-	TIM1_CH2
PE12	-	-	43	-	I/O	FT	PE12	-	TIM1_CH3N
PE13	-	-	44	-	I/O	FT	PE13	-	LQ FP
PE14	-	-	45	-	I/O	FT	PE14	-	TIM1_CH4
PE15	-	-	46	-	I/O	FT	PE15	-	TIM1_BKIN
PB10	21	29	47	-	I/O	FT	PB10	I^2C2_SCL/I^2C4_SCL/ USART3_TX(6)	TIM2_CH3
PB11	22	30	48	-	I/O	FT	PB11	I^2C2_SDA/I^2C4_SDA/ USART3_RX(6)	TIM2_CH4

V_{SS}_1	23	31	49	18	S	-	V_{SS}_1	-	-
V_{DD}_1	24	32	50	19	S	-	V_{DD}_1	-	-
PB12	25	33	51	-	I/O	FT	PB12	SPI2_NSS/I²C2_SMBAI/ USART3_CK(6)/TIM1_BKIN(6)	
PB13	26	34	52	-	I/O	FT	PB13	SPI2_SCK/USART3_CTS(6)/ TIM1_CH1N(7)/QSPI_IO0	
PB14	27	35	53	-	I/O	FT	PB14	SPI2_MISO/USART3_RTS(6)/ TIM1_CH2N(7)/QSPI_IO1	
PB15	28	36	54	-	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N(6)/ QSPI_IO2	-
PD8	-	-	55	-	I/O	FT	PD8	QSPI_IO3	USART3_TX
PD9	-	-	56	-	I/O	FT	PD9	-	USART3_RX
PD10	-	-	57	-	I/O	FT	PD10	QSPI_CLK	USART3_CK
PD11	-	-	58	-	I/O	FT	PD11	-	USART3_CTS
PD12	-	-	59	-	I/O	FT	PD12	QSPI_SS_N	TIM4_CH1/ USART3_RTS
PD13	-	-	60	-	I/O	FT	PD13	-	TIM4_CH2
PD14	-	-	61	-	I/O	FT	PD14	-	TIM4_CH3
PD15	-	-	62	-	I/O	FT	PD15	-	TIM4_CH4
PC6	-	37	63	-	I/O	FT	PC6	-	TIM3_CH1
PC7	-	38	64	-	I/O	FT	PC7	-	TIM3_CH2
PC8	-	39	65	-	I/O	FT	PC8	-	TIM3_CH3
PC9	-	40	66	-	I/O	FT	PC9	-	TIM3_CH4
PA8	29	41	67	20	I/O	FT	PA8	USART1_CK/ TIM1_CH1(6)/MCO	-
PA9	30	42	68	21	I/O	FT	PA9	USART1_TX(6) /TIM1_CH2(6)	-
PA10	31	43	69	22	I/O	FT	PA10	USART1_RX(6)/ TIM1_CH3(6)	-
PA11	32	44	70	23	I/O	FT	PA11	USART1_CTS/ USBDM/USB2DM/ CAN_RX(6)/TIM1_CH4(6)	-
PA12	33	45	71	24	I/O	FT	PA12	USART1_RTS/ USBDP/USB2DP/ CAN_TX(6)/TIM1_ETR(6)	-
PA13	34	46	72	25	I/O	FT	JTMS/ SWDIO	-	PA13

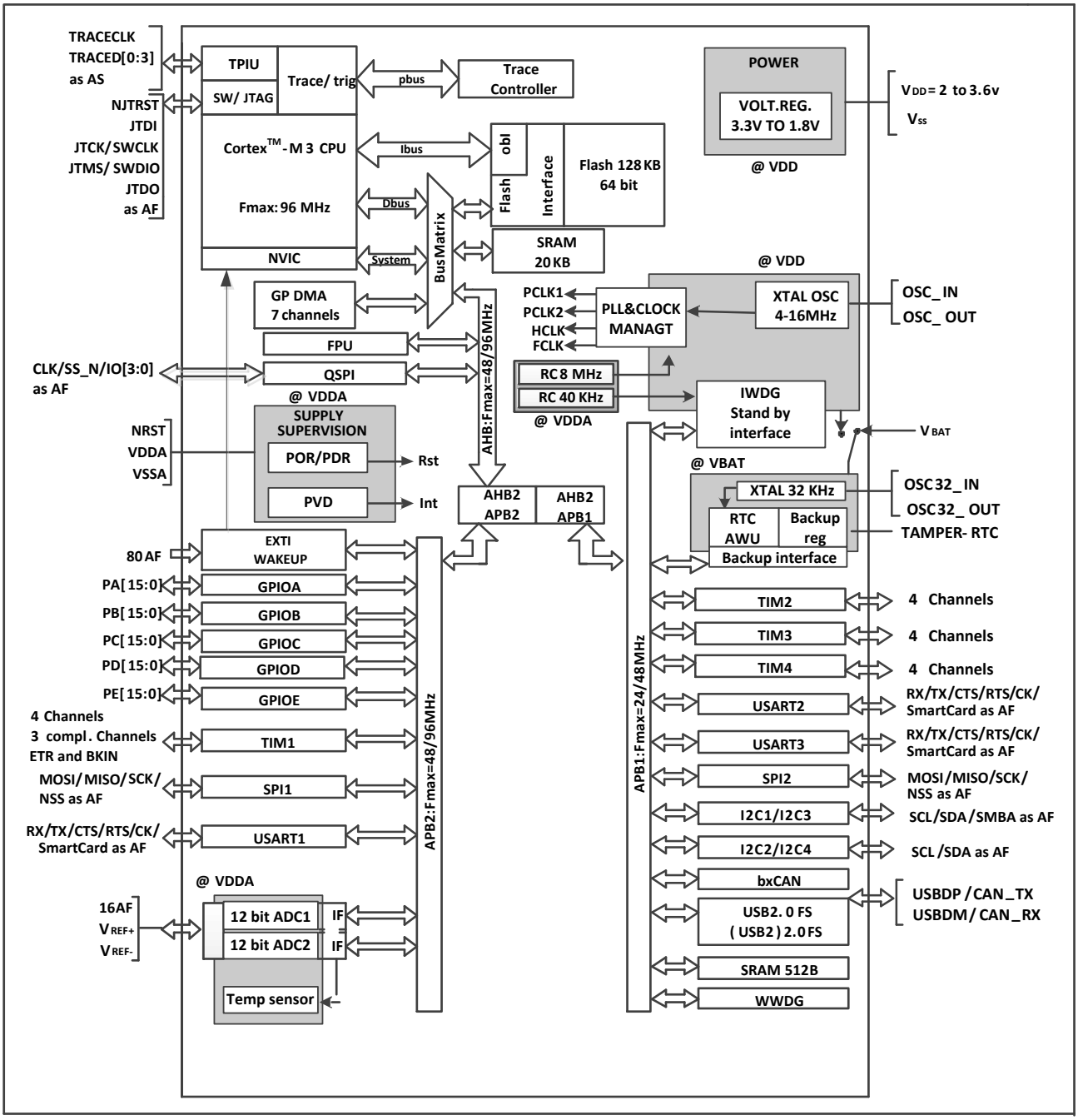
Disconnected	-	-	73	-	-	-	-	Disconnected	-
V_{SS}_2	35	47	74	26	S		V_{SS}_2	-	-
V_{DD}_2	36	48	75	27	S		V_{DD}_2	-	-
PA14	37	49	76	28	I/O	FT	JTCK/ SWCLK	-	PA14
PA15	38	50	77	29	I/O	FT	JTDI	-	TIM2_CH1_ETR/PA15/ SPI1_NSS
PC10	-	51	78	-	I/O	FT	PC10	-	USART3_TX
PC11	-	52	79	-	I/O	FT	PC11	-	USART3_RX
PC12	-	53	80	-	I/O	FT	PC12	-	USART3_CK
PD0	-	-	81	2	I/O	FT	PD0	-	CAN_RX
PD1	-	-	82	3	I/O	FT	PD1	-	CAN_TX
PD2	-	54	83	-	I/O	FT	PD2	TIM3_ETR	-
PD3	-	-	84	-	I/O	FT	PD3	-	USART2_CTS
PD4	-	-	85	-	I/O	FT	PD4	-	USART2_RTS
PD5	-	-	86	-	I/O	FT	PD5	-	USART2_TX
PD6	-	-	87	-	I/O	FT	PD6	-	USART2_RX
PD7	-	-	88	-	I/O	FT	PD7	-	USART2_CK
								-	PB3/ TRACESWO TIM2_CH2/ SPI1_SCK
PB3	39	55	89	30	I/O	FT	JTDO		
PB4	40	56	90	31	I/O	FT	NJTRST	-	PB4/ TIM3_CH1/ SPI1_MISO
PB5	41	57	91	32	I/O	-	PB5	I^2C1_SMBAI	TIM3_CH2/ SPI1_MOSI
PB6	42	58	92	33	I/O	FT	PB6	$I^2C1\_SCL^{(6)}$ /I^2C3_SCL/ $TIM4\_CH1^{(7)}$	USART1_TX
PB7	43	59	93	34	I/O	FT	PB7	$I^2C1\_SDA^{(6)}$ /I^2C3_SDA/ $TIM4\_CH2^{(6)}$	USART1_RX
BOOT0	44	60	94	35	I	-	BOOT0	-	-
PB8	45	61	95	-	I/O	FT	PB8	$TIM4\_CH3^{(6)}$	I^2C1_SCL/ (I^2C3_SCL/ CAN_RX

PB9	46	62	96	-	I/O	FT	PB9	TIM4_CH4(6)	I²C1_SDA (I²C3_SDA) / CAN_TX
PE0	-	-	97	-	I/O	FT	PE0	TIM4_ETR	-
PE1	-	-	98	-	I/O	FT	PE1	-	-
V_{SS}_3	47	63	99	36	S	-	V_{SS}_3	-	-
V_{DD}_3	48	64	100	1	S	-	V_{DD}_3	-	-

1. I = input, O = output, S = supply, HiZ = high resistance
2. FT = 5V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively.
4. PC13, PC14 and PC15 are supplied through the power switch since the switch only sinks a limited amount of current (3mA). The use of GPIOs from PC13 to PC15 in output mode is limited: only one GPIO can be used at a time, the speed should not exceed 2 MHz with a maximum load of 30pF and these IOs must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
6. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate Function I/O and Debug Configuration section in the reference manual.
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48, UFQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate Function I/O and Debug Configuration section in the reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

2.3 System Diagram

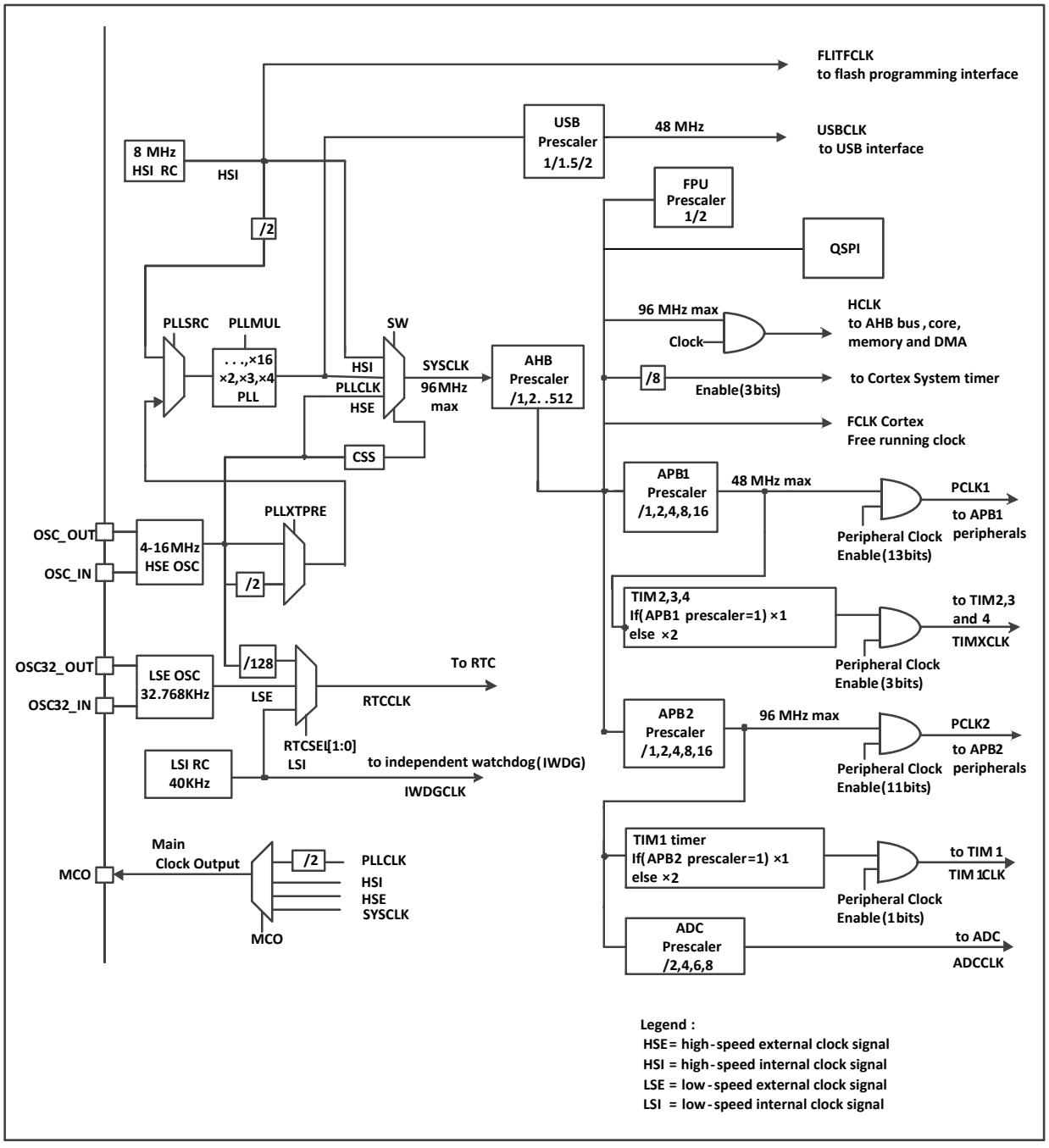
Figure 5 APM32F103x4x6x8xB/APM32E103xB Series System Diagram



1. The max frequency for APM32F103x8xBx4x6 series AHB and high-speed APB is 72MHz, while it is 96MHz for APM32E103x8xBx4x6 series;
2. The max frequency for APM32F103x8xBx4x6 series low-speed APB clock is 36MHz, while it is 48MHz for APM32E103x8xBx4x6 series low-speed APB clock.

2.4 Clock Tree

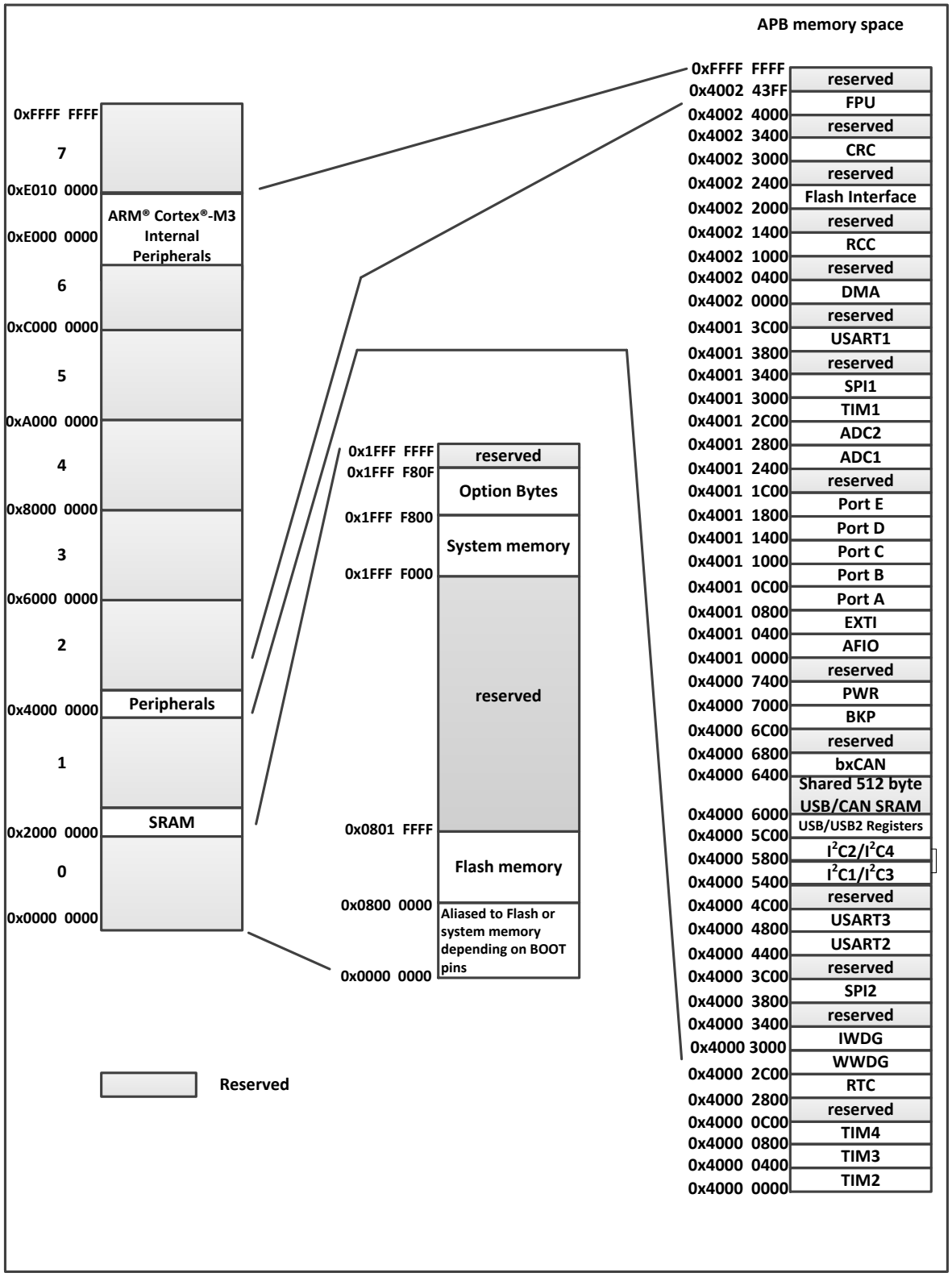
Figure 6 APM32F103x4x6x8xB/APM32E103xB Series Clock Tree



1. The max frequency for APM32F103x8xBx4x6 series AHB and high-speed APB is 72MHz, while it is 96MHz for APM32E103x8xBx4x6;
2. The max frequency for APM32F103x8xBx4x6 series low-speed APB clock is 36MHz, while it is 48MHz for APM32E103x8xBx4x6 series low-speed APB clock.

2.5 Address Mapping

Figure 7 APM32F103x4x6x8xB/APM32E103xB Series Address Mapping Diagram



3 Features Description

3.1 ARM®Cortex®-M3 Core

Built-in ARM®Cortex®-M3 core, working frequency of 96MHz, be compatible with ARM tools and software

System diagram for APM32F103x4x6x8xB/APM32E103xB series is shown as Figure 5.

3.2 Memory

128 Kbytes of embedded Flash is available for storing programs and data.

20 Kbytes of embedded static memory can be accessed in bytes, halfwords (16 bits) or full words (32 bits).

3.3 Power Management

3.3.1 Power Supply Schemes

- V_{DD} =2.0～3.6V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V^{DDA} is 2.4 V when the ADC is used). V_{DDA} and V^{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: See more details on how to connect power pins in Figure 11.

3.3.2 Voltage Regulator

The voltage regulator can adjust the working mode of the MCU to reduce power consumption. There are three operation modes:

- Main Mode (MR): provides 1.6V power (core, memory, peripherals) in normal regulation mode;
- Low Power Mode (LPR): provides a 1.6V supply in low power mode to preserve the contents of registers and SRAM;

- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost);

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

3.3.3 Power Supply Supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation when V_{DD} reaches the set threshold $V_{POR/PDR}$. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to Chapter 5 Electrical for the values of $V_{POR/PDR}$ and $_{VPVD}$.

3.3.4 Low Power Mode

The product supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep Mode: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop Mode: The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.6V domain are stopped, the HSE, HSI, and PLL clocks are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.
- Standby Mode: The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.6 V domain is powered off. The PLL, the HSI RC and the HSE clocks are also switched

off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering stop or standby mode. QSPI interrupts cannot wake up low power mode

3.4 Clocks and Startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 96 MHz. The maximum allowed frequency of the low-speed APB domain is 48 MHz. See Figure 6 for details on the clock tree.

3.5 RTC and Backup Registers

The Real-Time Clock(RTC) provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the

V_{BAT} pin.The RTC and the backup registers are not reset by the system or power reset source; they are not reset when waking up from standby mode.

3.6 Boot Modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

3.7 CRC (Cyclic Redundancy Check) Calculation Unit

The CRC (Cyclic Redundancy Check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.8 Nested Vectored Interrupt Controller (NVIC)

- It can handle 16 priority levels and maskable interrupt channels simultaneously. The closely coupled NVIC gives low-latency interrupt processing.
- Interrupt entry vector table address passed directly to the core
- Allow early processing of interrupts.
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state is automatically saved.
- Interrupt entry restored on interrupt exit with no instruction overhead
- This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. Up to 80 GPIOs can be connected to the 16 external interrupt lines. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period.

3.10 Floating Point Unit (FPU)

The product has a embedded independent FPU floating-point arithmetic processing unit that supports the IEEE754 standard and supports single-precision floating-point operations.

3.11 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and advanced-control timers TIMx and ADC.

3.12 System Tick Timer and Watchdog

The product includes an advanced-control timer (TIM1), three general-purpose timers (TIM2/3/4), an independent watchdog timer, a window watchdog timer, and a SysTicktimer.

The following table compares the features of the advanced-control and general-purpose timers:

Table 3 Timer Feature Comparison

Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request generation	Capture/Compare Channels	Complementary Outputs

TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2 TIM3 TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No

3.12.1 Advanced-control Timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.12.2 General-purpose Timers (TIM2/3/4)

There are three synchronizable general-purpose timers embedded in the devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

3.12.3 Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC oscillator and as it operates independently from the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.12.4 Window Watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12.5 SysTick Timer (Sys Tick Timer)

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- 24-bit down counter
- Automatic reload function
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.13 Communication Interface

3.13.1 I^2C Bus

Two embedded I^2C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes. They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded. They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.13.2 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

Three USART communication interfaces are embedded, providing hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability. One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. All USART interfaces can be served by the DMA controller.

3.13.3 Serial Peripheral Interface (SPI)

Two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes while the frame is configurable to 8 bits or 16 bits. Both SPIs can be served by the DMA controller.

3.13.4 Quad SPI Controller (QSPI)

The product has a embedded QSPI dedicated communication interface that can be connected to external flash via single, dual or quad SPI mode, supporting 8-bit, 16-bit and 32-bit access. There are 8 bytes of transmit FIFO and 8 bytes of receive FIFO.

3.13.5 Controller Area Network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.13.6 Universe Serial Bus (USB)

The product embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.13.7 Simultaneous Use of USB Interface and CAN Interface:

When USB and CAN are used together, you need to:

- Write 0x00000001 at the base address offset 0x100 of the USB.

- The PA11 and PA12 pins are for USB and CAN is used to multiplex other pins.

3.14 General-purpose Input Output Interface (GPIO)

The product can be up to 80 GPIO pins, each of the GPIOs can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers. I/Os on APB2 with up to 18 MHz toggling speed.

3.15 ADC (Analog/Digital Converter)

Two 12-bit analog-to-digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

3.16 Temperature Sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.17 Debug Interface (SWJ-DP)

The product supports serial debug interface (SW-DP) and JTAG (JTAG-DP) debug interface.

The JTAG interface provides a 5-pin standard JTAG interface for the AHB access port.

The SW-DP interface provides a 2-pin (data + clock) interface to the AHB module.

The two pins of the SW-DP interface and the five pins of the JTAG interface are multiplexed.

4 Electrical Features

4.1 Parameter Conditions

All voltage parameters are referenced to V_{SS} unless otherwise specified.

4.1.1 Maximum and Minimum Values

Unless otherwise stated, all minimum and maximum values are guaranteed on the production line by testing 100% of the product at ambient temperature T_A=25°C under worst ambient temperature, supply voltage and clock frequency conditions.

Take notes in every table that the data got for passing the comphensive evaluation, design simulation or process features will not be tested on production lines. Basing on the comprehensive evaluation and sample tested, the minimum and maximum values come from the average value's plus or subtract its triple value on the standard distribution (average ±3Σ).

4.1.2 Typical Value

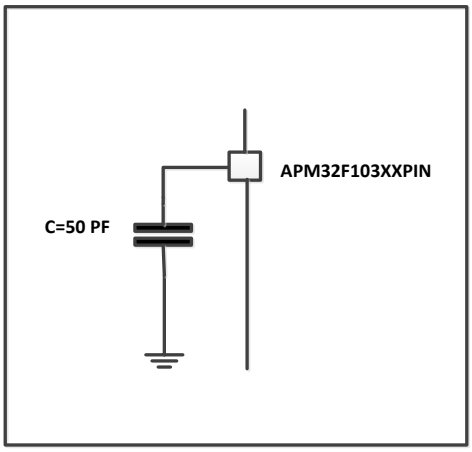
Typical data is based on T_A =25°C and V_{DD} =3.3V (2 V ⩽ V_{DD} ⩽ 3.3 V voltage range) unless otherwise stated. These data are for design guidance only.

4.1.3 Typical Curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

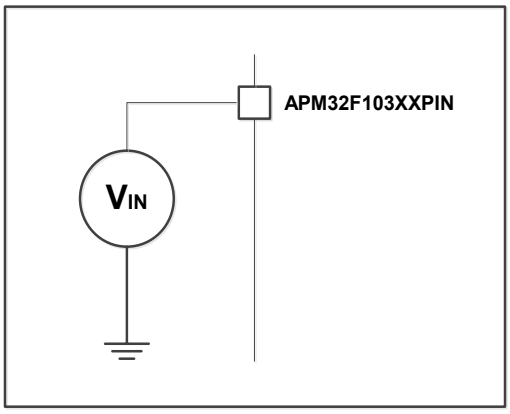
4.1.4 Load Capacitance

Figure 8 Load Conditions When Measuring Pin Parameters



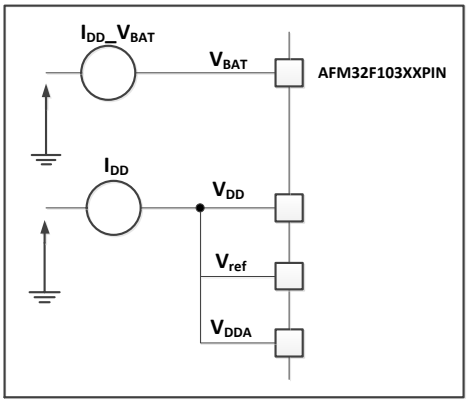
A: load capacitance

Figure 9 Pin Input Voltage Measurement Scheme



B: Pin Input Voltage

Figure 10 Current Consumption Measurement Scheme



C: Current consumption measurement (I_{DD}+V_{ref})

4.2 Absolute Maximum Ratings

Loads applied to the device may cause permanent damage to the device if the absolute maximum ratings are given in the maximum rated voltage Features and maximum rated current Features. This is just to give the maximum load that can be tolerated, and does not mean that the functionality of the device is functioning properly under these conditions. The reliability of device would be affected if it works under the maximum load conditions for a long time.

4.2.1 Maximum Rated Voltage Features

Table 4 Maximum Rated Voltage Features

Symbol	Description	Minimum	Maximum	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins (2)	V_{SS}-0.3	5.5	
	Input voltage on other pins(2)	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply pins		50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different ground pins		50	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to a power supply within the external allowable range.
2. If V_{IN} does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If V_{IN} exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When V_{IN} > V_{DD}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current.

4.2.2 Maximum Rated Current Features

Table 5 Maximum Rated Current Features

Symbol	Description	Maximum	Unit
I_{VDD}	Total current (supply current) (1) went through the V_{DD}/V_{DDA} power cord.	150	mA
I_{VSS}	Total current (outflow current) (1) went through the V_{SS} ground cord.	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2) (3)	Injection current of NRST pin	±5	
	Injection current of HSE's OSC_IN pin and LSE's OSC_IN pin	±5	
	Injection current of other pins	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (4)	±25	

1. All power (V_{DD}，V_{DDA}) and ground (V_{SS}，V_{SSA}) pins must always be connected to a power supply within the external allowable range.
2. If V_{IN} does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If VIN exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.
3. Reverse injection current can interfere with the analog performance of the ADC.
4. When several I/O ports have injection current at the same time, the maximum value of$\Sigma I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of $\Sigma I_{INJ(PIN)}$ on the four I/O port pins of the device.

4.2.3 Ultimate Destructive Test

Table 6 Temperature Features

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-55 ~ + 150	°C
T_J	Maximum junction temperature	150	°C

Table 7 Electrostatic Discharge (ESD) (1)

Symbol	Parameters	Conditions	Maximum value (1)	Unit

$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 °C	1000	

1. The sample is measured by a third-party testing agency and is not tested in production.

Table 8 Static Latch (1)

Symbol	Parameters	Conditions	Type
LU	Static latch	T_A = +25 °C/105°C	±200mA

1. The sample is measured by a third-party testing agency and is not tested in production.

4.3 Test Under the General Working Conditions

Table 9 General Working Conditions

Symbol	Parameters	Conditions	Min value	Max value	Unit
f_{HCLK}	Internal AHB clock frequency		0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	48	
f_{PCLK2}	Internal APB2 clock frequency		0	96	
V_{DD}	Standard working voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	must be the same with V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC not used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.6	3.6	V

1. When the ADC is used, refer to Chapter 4.3.11.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

4.3.1 Embedded Reset and Power Control Block Features (1)

Table 10 Embedded Reset and Power Control Block Features (T_A=25℃)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{PVD}(3)	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threhold	Falling edge	1.6(1)	1.88	1.96	V
		Rising edge	1.85	1.93	2.01	V
$V_{PDRhyst}$ (2)	PVD hysteresis			50		mV

1. The product feature is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. It is guaranteed by design, and is not tested in production.
3. It is derived from a comprehensive evaluation and is not tested in production.

4.3.2 Built-in Reference Voltage Features Test

Table 11 Built-in Reference Voltage

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REFINT}(1)	Internal reference voltage	-40°C < T_A < +105°C V_{DD}= 2-3.6 V	1.17	1.21	1.25	V
$T_{S\_vrefint}$(2)	ADC sampling time when reading the internal reference voltage			5.1	17.1	μs

1. It is derived from a comprehensive evaluation and is not tested in production.
2. It is guaranteed by design, and is not tested in production.

4.3.3 Supply Current Features

The current values in the operating modes given in this section are measured by executing Dhrystone 2.1, the compilation environment is Keil V5, and the compilation optimization level is L0.

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level –V_{DD} or V_{SS} (no load).
- All peripherals are turned off unless otherwise stated.
- The access time of the flash memory is adjusted to the frequency f_{HCLK} (0~24MHz - 0 wait cycles, 24~48MHz - 1 wait cycle, 48~72MHz - 2 wait cycles, 96MHz - 3 wait cycles).
- The instruction prefetch function is turned on (hint: this setting must be made before the clock setting and bus division).
- When the peripheral is turned on: $fp_{CLK1} = f_{HCLK}/2$，$fp_{CLK2} = f_{HCLK}$.

Figure 11 Power Supply Scheme

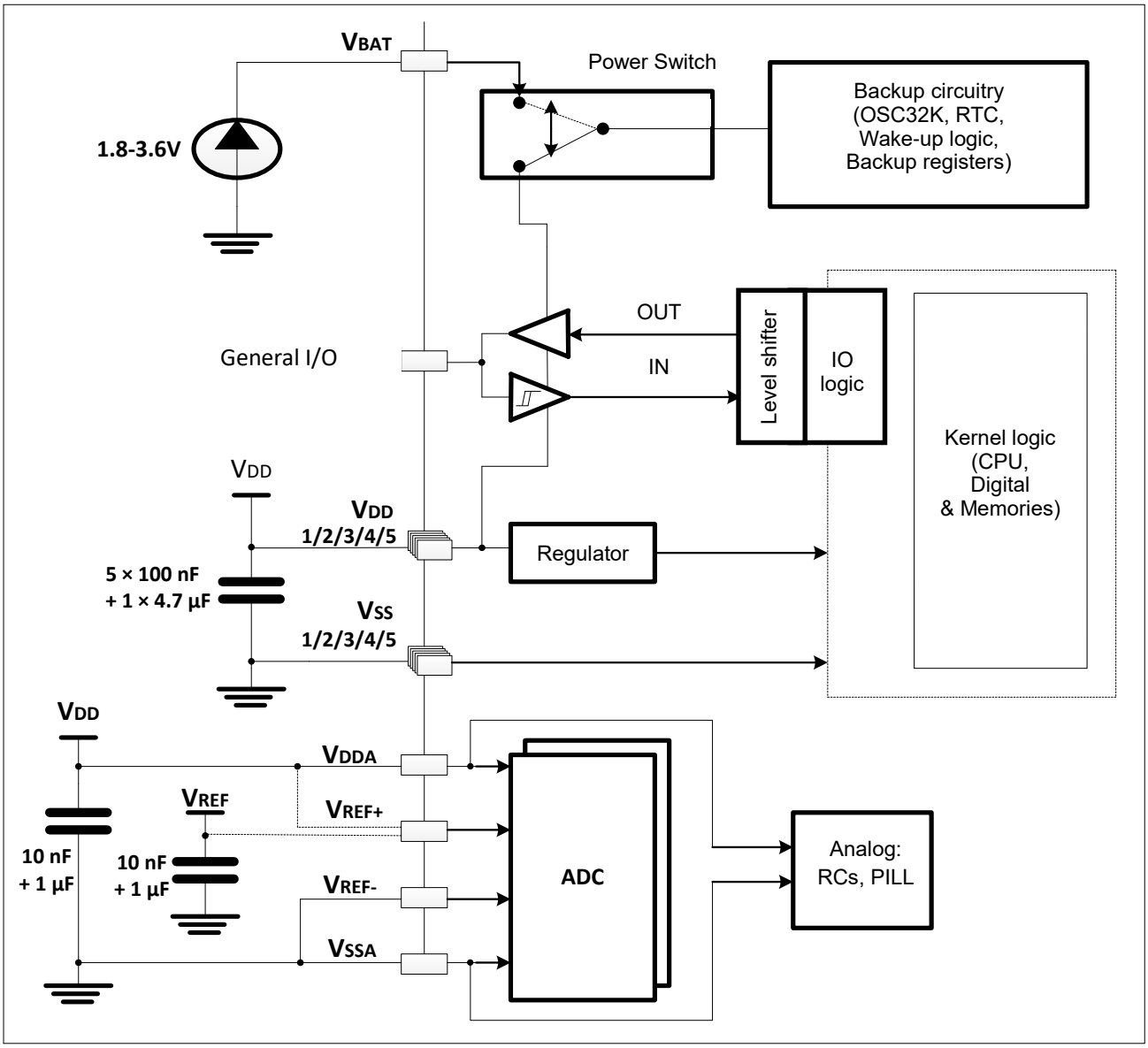


Table 12 Run-mode Current Consumption, Code with Data Processing Running From Internal Flash

Symbol	Parameters	Conditions	f_{HCLK}	Typical Value(1)		Unit
				T_A =25°C V_{DD}=3.6 V	T_A =105°C V_{DD}=3.6 V	
I_{DD}	Supply current in operating mode	External clock (2), enabling all peripherals	96 MHz	29.38	30.42	mA
			72MHz	24.53	25.4	
			48MHz	18.73	19.46	
			36MHz	14.29	14.85	
			24MHz	10.80	11.35	
			16MHz	7.52	7.97	
			8MHz	4.14	4.41	
		External clock (2), turn off all peripherals	96 MHz	19.17	19.62	
			72MHz	16.84	17.33	
			48MHz	13.51	14.04	
			36MHz	10.31	10.76	
			24MHz	8.17	8.68	
			16MHz	5.91	6.34	
			8MHz	3.30	3.59	

1. It is derived from a comprehensive evaluation and is not tested in production.

2. When the external clock is 8MHz and f_{HCLK}>8MHz, it enables PLL.

Table 13 Run-mode Current Consumption, Code with Data processing Running From Iternal RAM

Symbol	Parameters	Conditions	f_{HCLK}	Typical Value(1)		Unit
				T_A =25°C V_{DD}=3.6 V	T_A =105°C V_{DD}=3.6 V	
I_{DD}	Supply current in operating mode	External clock(2), enabling all peripherals	96 MHz	26.4	27.26	mA
			72MHz	20.24	20.71	
			48MHz	13.83	14.16	
			36MHz	10.57	10.87	
			24MHz	7.34	7.61	
			16MHz	5.18	5.43	
			8MHz	2.98	3.23	
		External clock (2), turn off all peripherals	96 MHz	15.9	16.42	
			72MHz	12.14	12.58	
			48MHz	8.41	8.77	
			36MHz	6.49	6.81	
			24MHz	4.62	4.91	
			16MHz	3.34	3.62	
			8MHz	2.98	3.17	

1. It is derived from a comprehensive evaluation and is not tested in production.

2. When the external clock is 8MHz and f_{HCLK}>8MHz, it enables PLL.

Table 14 Current Consumption in Sleep Mode, Code Runs from Flash or RAM

Symbol	Parameters	Conditions	f_{HCLK}	Typical Value		Unit
				T_A =25°C V_{DD}=3.6 V	T_A =105°C V_{DD}=3.6 V	
I_{DD}	Static Current during Sleep Mode	External clock (2), enabling all peripherals	96 MHz	16.78	17.09	mA
			72MHz	12.82	13.08	
			48MHz	8.84	9.06	
			36MHz	6.83	7.04	
			24MHz	4.84	5.05	
			16MHz	3.51	3.7	
			8MHz	2.17	2.36	
		External clock (2), turn off all peripherals	96 MHz	4.85	5.08	
			72MHz	3.86	4.06	
			48MHz	2.84	3.04	
			36MHz	2.28	2.48	
			24MHz	1.81	2.00	
			16MHz	1.49	1.68	
			8MHz	1.15	1.35	

1. It is derived from a comprehensive evaluation and is not tested in production.

2. When the external clock is 8MHz and f_{HCLK} >8MHz, it enables PLL.

Table 15 Typical and Maximum Current Consumption in Stop Mode and Standby Mode

Symbol	Parameters	Conditions	Typical Value (T_A =25°C)			Max Value (T_A =105°C)	Unit
			V_{DD} = 2.4V	V_{DD} = 3.3V	V_{DD} = 3.6V	V_{DD}=3.6 V	
I_{DD}	Supply current in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	22.4	24.7	25.8	140	μA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	10.3	12.5	13.6	120	
	Supply current in standby mode	Low-speed internal RC oscillator and independent watchdog ON	3.6	6.2	7.6	50	
		Low-speed internal RC oscillator is on, independent watchdog OFF	3.4	6.0	7.3	48	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.8	5.1	6.3	45	
I_{DD_VBAT}	Supply current in the backup area	Low-speed oscillator and RTC ON	1.2	1.5		2.5	

1. It is derived from a comprehensive evaluation and is not tested in production.

4.3.4 External Clock Source Features

High-speed External Clock Generated From Crystal/Ceramic Resonator

For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 16 HSE 4~16MHz Oscillator Features(1)(2)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{OSC_IN}	Oscillator Frequency:		4	8	16	MHz

R_F	Feedback Resistance			300		kΩ
C_{L1}& C_{L2}(3)	Recommended load capacitance and corresponding crystal serial impedance (RS) (4)	RS = 30kΩ		30		pF
i_2	HSE drive current	V_{DD}=3.3V，V_{IN}=V_{SS} 30pF load			1	mA
$t_{SU(HSE)}$(5)	Startup Time	V_{DD} is stable		2		ms

1. The features parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. It is derived from a comprehensive evaluation and is not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high quality ceramic capacitors (typically) between 5pF and 25pF for high frequency applications. Select the capacitor value to meet the requirements of the crystal or resonator. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers typically give the parameters of the load capacitance in a serial combination of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the pin and PCB capacitance can be roughly estimated at 10pF).
4. Relatively low RF resistance provides protection against problems caused by changes in leakage and bias conditions when used in wet conditions. However, if the MCU is used in a harsh wet environment, this factor needs to be taken into account when designing.
5. $t_{SU(HSE)}$ is the start-up time, which is measured from the time the software enables the HSE until a stable 8 MHz oscillation is obtained. This value is measured using a standard crystal resonator, which may vary greatly depending on the crystal manufacturer.

Low-speed External Clock Generated From the Crystal/Ceramic Resonator

For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 17 LSE Oscillator Features (f_{LSE} =32.768KHz) (1)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
RF	Feedback Resistance			7		MΩ
C_{L1} & C_{L2}(2)	Recommended load capacitance and corresponding crystal serial impedance (R_S) (3)	R_S = 30kΩ			15	pF
i_2	LSE drive current	V_{DD} = 3.3V, V_{IN}=V_{SS}			1.4	μA
$t_{SU(LSE)}$(4)	Start Time	V_{DD} is stable		3		s

1. It is derived from a comprehensive evaluation and is not tested in production.

2. See the tips and warnings section below this table.

3. Use a high quality oscillator with a small R_S value (such as MSIV-TIN32.768kHz) to optimize current consumption. Please consult the crystal manufacturer for details.

4. $t_{SU(LSE)}$ is the startup time, which is measured from the software enable LSE until a stable 32.768 MHz oscillation is obtained. This value is measured using a standard crystal resonator, which may vary greatly depending on the crystal manufacturer.

Tip: For C_{L1} and C_{L2}, it is recommended to use a high quality ceramic capacitor between 5pF and 15pF and select the capacitance value to meet the requirements of the crystal or resonator. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers typically give the parameters of the load capacitance in a serial combination of C_{L1} and C_{L2}. Load capacitance CL has the following formula:CL-C_{L1} x C_{L2}/(C_{L1} + C_{L2}) + C_{stray} where C_{stray} is the pin capacitance and board or trace PCB-related capacitance, Typically, it is between 2 pF and 7 pF.

To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance CL≤7pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of CL=6 pF, and C_{stray} = 2 pF, then C_{L1}= C_{L2}=8 pF

4.3.5 Internal Clock Source Features

High Speed Internal (HSI) RC Oscillator Test

Table 18 HSI Oscillator Features(1)

Symbol	Parameters	Conditions		Minimum Value	Typical Value	Maximum Value	Unit
f_{HSI}	Frequency				8		MHz
ACC_{HSI}	HSI oscillator accuracy	Factory calibration	T_A=-25°C V_{DD} = 3.3V	-1		1	%
			T_A=-40~105°C V_{DD} = 3.3V	-3.2		2.7	%
			T_A =25°C V_{DD} = 2-3.6V	-1.1		3.6	%
$t_{SU(HSI)}$	HSI oscillator startup time	V_{DD} = 3.3V T_A =-40~105°C		0.8		2	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	V_{DD} = 3.6V T_A =-40~105°C					μA

1. It is derived from a comprehensive evaluation and is not tested in production.

Low Speed Internal (LSI) RC Oscillator Test

Table 19 LSI Oscillator Features (1)

Symbol	Parameters	Minimum Value	Typical Value	Maximum Value	Unit
f_{LSI}	Frequency (V_{DD} = 2-3.6V，T_A = -40~105°C)	30	40	60	KHz
$t_{SU(LSI)}$	LSI oscillator startup time (V_{DD} = 3.3V，T_A = -40~105°C)			100	μs
$I_{DD(LSI)}$	LSI oscillator power consumption (V_{DD} = 3.6V，T_A = -40~105°C)		1	1.5	μA

1. It is derived from a comprehensive evaluation and is not tested in production.

Wake Up Time in Low Power Mode

The time values in the table are all a wake-up clock source from an 8MHz HSI RC oscillator and measured during its wake-up phase. The wake-up clock source is deteremined by current working mode:

- Stop or standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock set when entering sleep mode

Table 20 Wake Up Time in Low Power Mode

Symbol	Parameters	Typical Value	Unit
$t_{WUSLEEP}$(1)	Wake up from sleep mode	1.6	μs
t_{WUSTOP}(1)	Wake up from stop mode (regulator is in running-mode)	3.6	μs
	Wake-up from stop mode (regulator is low power mode)	5	
$t_{WUSTDBY}$(1)	Wake-up from standby mode	32	μs

1.The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

4.3.6 PLL Features

Table 21 PLL Features

Symbol	Parameters	Value			Unit
		Minimum Value	Typical Value	Maximum Value (1)	
f_{PLL_IN}	PLL Input clock (2)	2	8	25	MHz
	Input Clock Duty Cycle	40		60	%

f_{PLL_OUT}	PLL multiplier output clock (V_{DD} = 3.3V，T_A = -40~105°C)	16		96	MHz
t_{LOCK}	PLL lock time			200	μs

1. It is derived from a comprehensive evaluation and is not tested in production.
2. Note that the appropriate multiplication factor is used so that the PLL input clock frequency is consistent with the range determined by f_{PLL_OUT}.

4.3.7 Memory Features

FLASH Memory

Table 22 FLASH Memory Features (1)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
t_{prog}	16-bit programming time	T_A = -40~105°C V_{DD}=2.4~3.6V	17.2	18.3	19.7	μs
t_{ERASE}	Page (1K bytes) erase time	T_A = -40~105°C V_{DD}=2.4~3.6V	1.3	1.43	1.55	ms
t_{ME}	Whole erase time	T_A = 25°C V_{DD}=3.3V			6	ms
V_{prog}	Programmable voltage	T_A = -40~105°C	2.1	3.3	3.6	V

1. It is derived from a comprehensive evaluation and is not tested in production.

Table 23 FLASH Memory Life and Data Retention Period

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
N_{END}	Number of erase cycles	T_A = -40~105°C	100			Thousand times cycle
t_{RET}	Data Retention Period	T_A = 55°C	10			Years

1. It is derived from a comprehensive evaluation and is not tested in production.

4.3.8 I/O Ports Features

Input/Output Static Features

Table 24 I/O Static Features (Test conditions V_{CC} = 2.7-3.6V, T_A = -40 ~ 105 ° C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IL}	Low level input voltage	TTL port			0.8	V

V_{IH}	Standard I/O pin, input high level voltage		2		V_{DD}+0.3	
	FT I/O pin(1), input high level voltage		2		5.5	
V_{IL}	Input low level voltage	CMOS port			0.3V_{DD}	
V_{IH}	Input high level voltage		0.7V_{DD}		V_{DD}+0.3	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2))		100			mV
	FT I/O Schmitt trigger voltage hysteresis(2)		100			mV
I_{lkg}	Input leakage current(3)	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$ Standard I/O port			±1	μA
		V_{IN} = 5V, I/O FT			3	
R_{PU}	Weak pull-up equivalent resistance(4)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance (4)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance					pF

1. FT = 5V tolerant. To withstand voltages above V_{DD} +0.3, the internal pull-up or pull-down resistors must be turned off.
2. The hysteresis voltage of the Schmitt trigger switch level is derived from a comprehensive evaluation and is not tested in production.
3. If there is reverse current sinking on adjacent pins, the leakage current may be higher than the maximum.
4. The pull-up resistor is designed to be implemented as a true resistor in series with a controllable PMOS/NMOS switch.

Output Drive Current Test

The GPIO (General Purpose Input/Output Port) can sink or output up to ±8mA and can sink up to ±20mA (V_{OL}/V_{OH} reduction). In user applications, the number of I/Os capable of driving current must be limited so that the current consumed cannot exceed the absolute maximum rating:

- The sum of the currents sourced by all the I/O on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.

- The sum of the currents sunk by all the I/O on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output Voltage Test

Table 25 Output Voltage Features (test conditions V_{CC}=2.7-3.6V, T_A = -40~105°C)

Symbol	Parameters	Conditions	Minimum Value	Maximum Value	Unit
V_{OL}(1)	Output low level, when 8 pins simultaneously sink current	TTL port, I_{IO} = +8mA 2.7V < V_{DD} < 3.6V		0.4	V
V_{OH}(2)	Output high level, when 8 pins simultaneously output current		V_{DD} -0.4		
V_{OL}(1)	Output low level, when 8 pins simultaneously sink current	CMOS port, I_{IO} = +8mA 2.7V < V_{DD} < 3.6V		0.4	V
V_{OH}(2)	Output high level, when 8 pins simultaneously output current		2.4		
V_{OL}(1)(3)	Output low level, when 8 pins simultaneously sink current	I_{IO} = +20mA 2.7V < V_{DD} < 3.6V		1.3	V
V_{OH}(2)(3)	Output high level, when 8 pins simultaneously output current		V_{DD} -1.3(4)		

1. The current I_{IO} absorbed by I/O must always follow the absolute maximum rating requirements, while the sum of the I_{IO} s (all I/O and control pins) must not exceed I_{VSS}.
2. The current I_{IO} of the I/O output must always follow the absolute maximum rating requirements, while the sum of the I_{IO} s (all I/O and control pins) must not exceed I_{VDD}.
3. It is derived from a comprehensive evaluation and is not tested in production.
4. The driving capability of PC13-15 is not included in this item. The other PC port specifications are in the voltage range of 3.3V < V_{DD} < 3.6V.

Input and Output AC Features (T_A = 25°C)

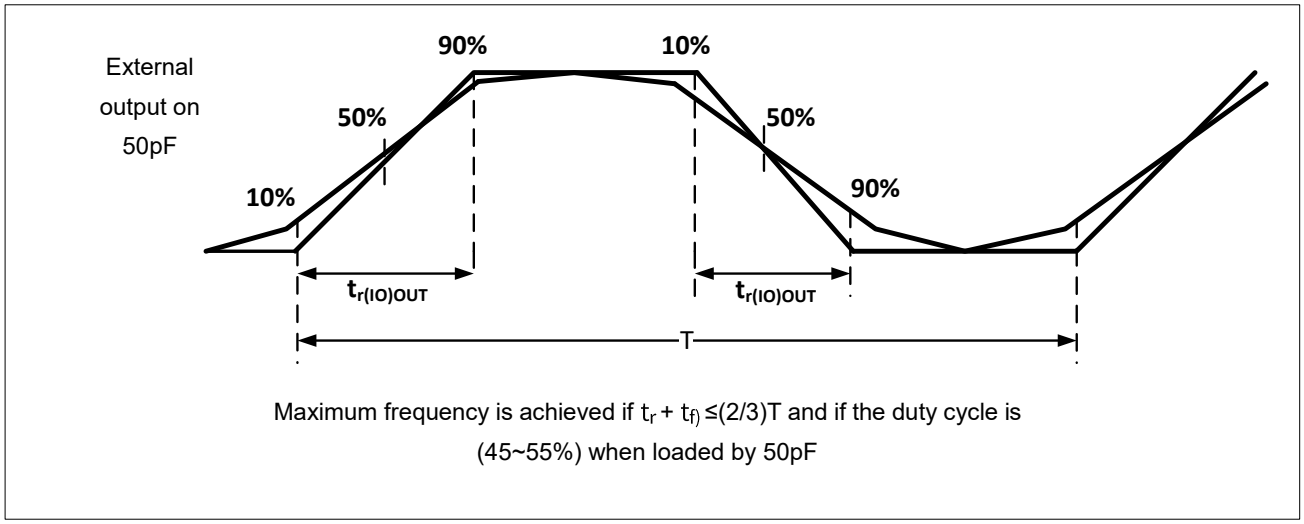
Table 26 Input and Output AC Features

MODEx[1:0] Configuration	Symbol	Parameters	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Max frequency(2)	C_L = 50 pF, V_{DD} = 2~3.6V		2	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L = 50 pF, V_{DD} = 2~3.6V		125(3)	ns
	$t_{r\ (IO)out}$	Output low to high rise time			125(3)	
01	$f_{max(IO)out}$	Max frequency(2)	C_L = 50 pF, V_{DD} = 2~3.6V		10	MHz

(10MHz)	$t_{f(IO)out}$	Output high to low fall time	C_L = 50 pF, V_{DD} = 2~3.6V		25(3)	ns
	$t_{r\ (IO)out}$	Output low to high rise time			28	
11 (50MHz)	$f_{max(IO)out}$	Max frequency(2)	C_L = 30 pF, V_{DD} = 2.7~3.6V		48.1	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L = 30 pF, V_{DD} = 2.7~3.6V		5(3)	ns
	$t_{r\ (IO)out}$	Output low to high rise time			5(3)	

1. The speed of the I/O port can be configured by MODEx[1:0].
2. The maximum frequency is defined in the figure below.
3. It is guaranteed by design and is not tested n production.

Figure 12 Input and Output AC Features Definition



4.3.9 NRST Pins Features

The NRST pin input driver is implemented in a CMOS process that is connected to a permanent pull-up resistor, R_{PU}.

Table 27 NRST Pin Features (Test condition V_{CC}=3.3V, T_A = -40~105°C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage				0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage		2			
$V_{hys(NRST)}$	NRST Schmitt trigger			400		mV

	voltage hysteresis					
R_{PU}	Weak pull-up equivalent resistance(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse				100	ns
$V_{NF(NRST)}$(1)	NRST input non-filter pulse		300			ns

1. It is guaranteed by design, and is not tested in production.
2. The pull-up resistor is implemented by a pure resistor in series with a turn-off PMOS/NMOS transistor. The PMOS/NMOS switch has a small resistance.

4.3.10 Communication Interface

I²C Interface Features

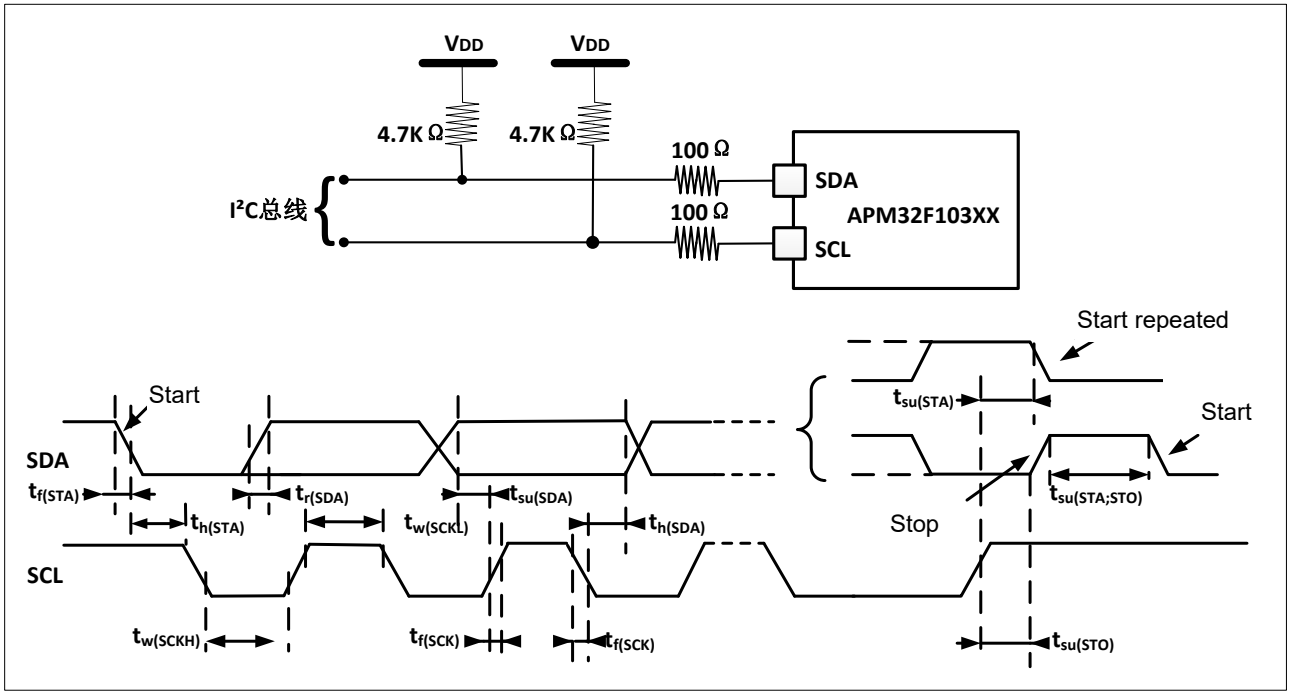
Table 28 I²C Interface Features (Test conditions V_{DD}=3.3V, T_A = 25°C)

Symbol	Parameters	Standard I²C(1)		Fast I²C(1) (2)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	Rise time for SDA and SCL		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	Fall time for SDA and SCL		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Repeated start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		μs
C_b	Capacitive load for each bus		400		400	pF

1. It is guaranteed by design, and is not tested in production.
2. For the bit to reach the maximum frequency of the standard mode I²C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I²C, f_{PCLK1} must be greater than 4MHz.

3. If you do not want to stretch the low time of the SCL signal, the maximum hold time of the start condition must be met.
4. In order to cross the undefined area of the falling edge of SCL, the SDA signal must be guaranteed to have a hold time of at least 300 ns inside the MCU.

Figure 13 Bus AC Waveform and Measurement Circuit (1)



1. Measured points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

SPI Interface Features

Table 29 SPI Features (V_{DD} = 3.3V, T_A = 25°C)

Symbol	Parameters	Conditions	Minimum Value	Maximum Value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI Clock Frequency	Master mode		18	MHz
		Slave Mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall times	Load capacitance: C=30pF	50	60	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	4_{tPCLK}		ns
$t_{h(NSS)}$ (2)	NSS hold Time	Slave mode	2_{tPCLK}		ns
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low time	Master mode, f_{PCLK} = 36MHz, presc=4	50	60	ns

$t_{su(MI)}^{(2)}$ $t_{su(SI)}^{(2)}$	Data input setup time	Master mode	5		ns
		Slave mode	5		
$t_{h(MI)}^{(2)}$ $t_{h(SI)}^{(2)}$	Data input hold time	Master Mode	5		ns
		Slave Mode	4		
$t_{a(SO)}^{(2)(3)}$	Data output access time	Slave mode, f_{PCLK}= 20MHz	0	3 t_{PCLK}	ns
$t_{dis(SO)}^{(2)(4)}$	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}^{(2)(1)}$	Data output valid time	Slave mode (after enable edge)		25	ns
$t_{v(MO)}^{(2)(1)}$	Data output valid time	Master mode (after enable edge)		14	ns
$t_{h(SO)}^{(2)}$	Data output hold time	Slave mode (after enable edge)	15		ns
$t_{h(MO)}^{(2)}$		Master mode (after enable edge)	2		

1. The SPI1 feature of the remap needs further determination.
2. It is derived from calculation and is not tested in production.
3. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time at which the data is valid.
4. The minimum value represents the minimum time to turn off the output, and the maximum value represents the maximum time to place the data line in a high impedance state.

Figure 14 SPI Timing Diagram - Slave Mode and CPHA=0

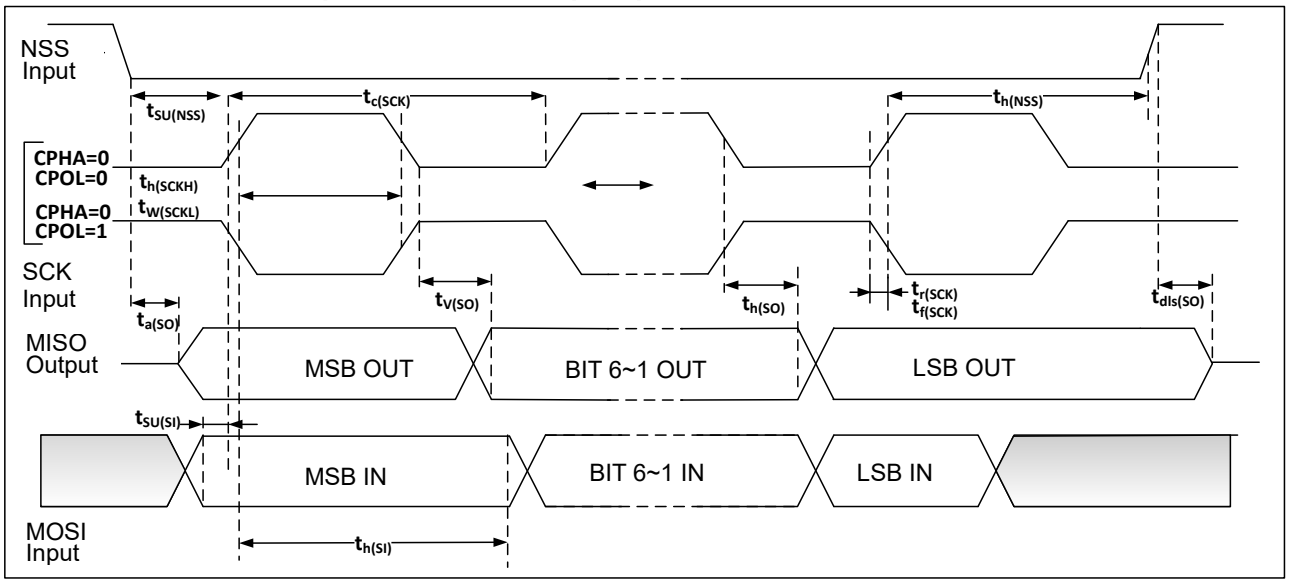
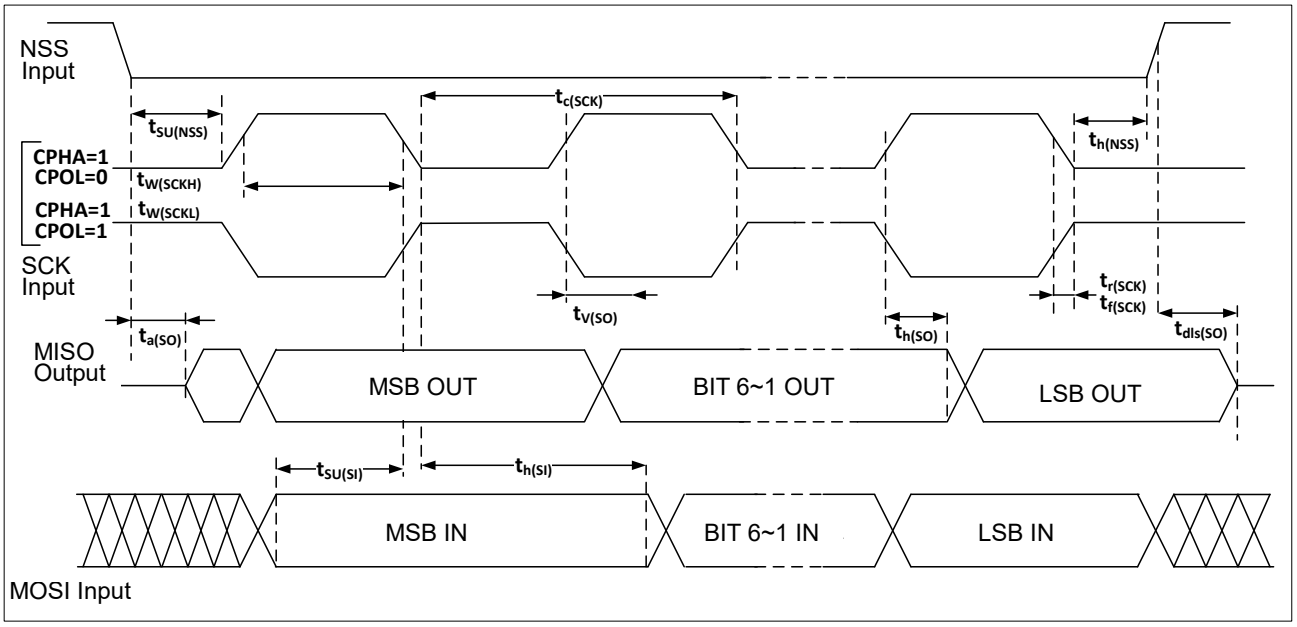
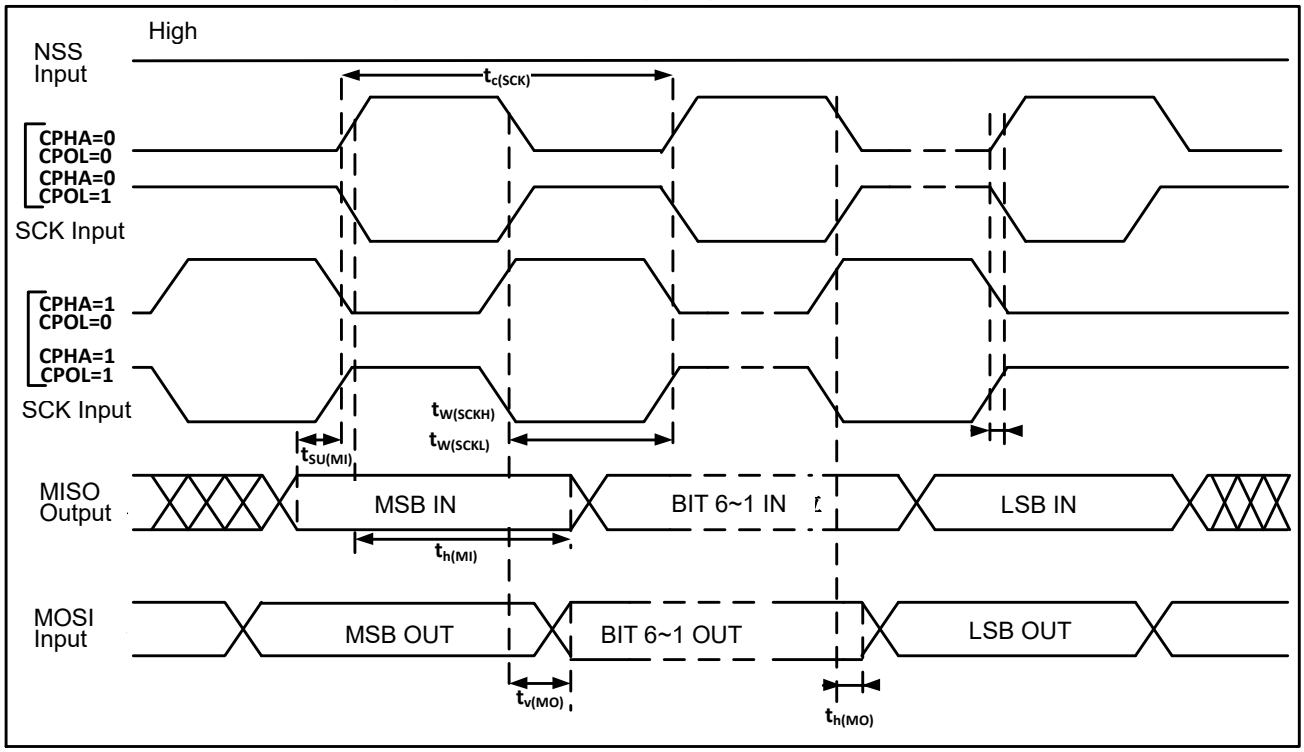


Figure 15 SPI Timing Diagram - Slave Mode and CPHA=1(1)



1. The measured points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 16 SPI Timing Diagram - Master Mode(3)



1. The measured points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

USB Interface Features

Figure 17 USB Timing: Data SignalRise and Fall Times Definition

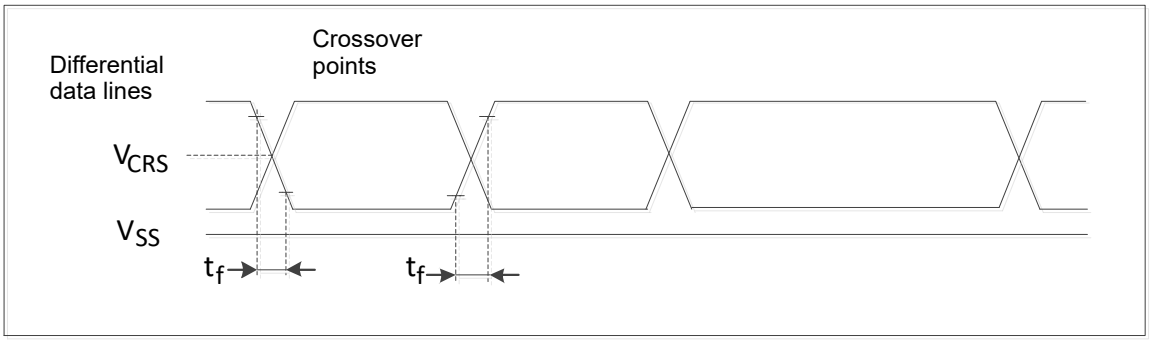


Table 30 USB Full Speed Electrical Features (V_{DD} = 3.0-3.6V, T_A = 25°C)

Symbol	Parameters	Conditions	Minimum Value	Maximum Value	Unit
t_r	Rise time	C_L = 50pF	4	20	ns
t_f	Fall time	C_L = 50pF	4	20	ns
t_{rfm}	Rise / fall time matching	t_r / t_f	90	110	%

4.3.11 12-bit ADC Features

Table 31 ADC Features (V_{DD} =2.4-3.6V, T_A =-40~105°C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on V_{REF+} input pin				20	μA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S	Sampling rate		0.05		1	MHz
V_{AIN}	Conversion voltage range		0		V_{REF+}	V
t_{CAL}	Calibration time	f_{ADC} = 14MHz	5.9			μs
			83			1/f_{ADC}
t_S	Sampling time	f_{ADC} = 14MHz	0.107		17.1	μs

			1.5		239.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (includes sampling time)	f_{ADC} = 14MHz	1		18	μs
			14~252(t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

4.3.12 Temperature Sensor Features

Table 32 Temperature Sensor Features

Symbol	Parameters	Minimum Value	Typical Value	Maximum Value	Unit
Avg_Slope(1)	Average slope (V_{DD} = 3.3V, T_A = -40~105°C)	3.6	4.2	4.9	mV/°C
V_{25}	Voltage at 25°C (V_{DD} =2.4-3.6V)	1.35	1.41	1.47	V
t_{START}(2)	Setup time	4		10	μs
T_{S_temp}(2) (3)	ADC sampling time when reading the temperature			17.1	μs

1. It is guaranteed by analysis on features, and is not tested in production.
2. It is guaranteed by design, and is not tested in production.
3. The shortest sampling time can be determined by the application through multiple iterations.

4.3.13 EMC Features

Sensitivity tests are sampled for testing during a comprehensive evaluation on the product.

Electromagnetic Sensitivity (EMS)

When running a simple application (controlling 2 LEDs flashing through the I/O port), the test sample is spurious electromagnetic interference until an error occurs, and LED flashing indicates an error.

Table 33 EMS Features

Symbol	Parameters	Conditions	Level
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance.	V_{DD} = 3.3V, T_A = +25 °C, f_{HCLK} = 72MHz, complies with IEC 61000-4-2	B
V_{EFTB}	Fast transit voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance.	V_{DD} = 3.3V, T_A = +25 °C, f_{HCLK} = 72MHz, complies with IEC 61000-4-4	B

Electromagnetic Interference (EMI)

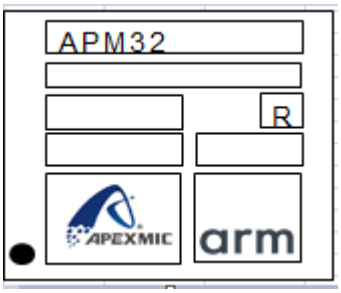
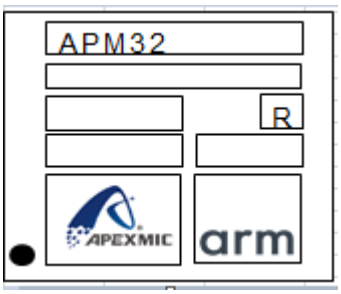
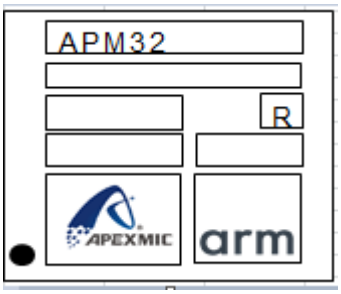
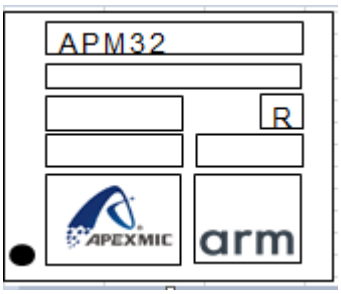
Monitor the electromagnetic field emitted by the chip while running a simple application (flashing 2 LEDs through the I/O port). This emission test complies with the SAE J1752/3 standard, which specifies the load on the test board and pins.

Table 34 EMI Features

Symbol	Parameters	Conditions	Detection frequency band	Maximum value (f_{HSE}/f_{HCLK})			Unit
				8/48MHz	8/72MHz	8/96MHz	
SEMI	Peak	V_{DD} = 3.3V, T_A = +25 °C, LQFP100 package	0.1-30MHz				dBμV
			30-130MHz	5.59			
			130MHz-1GHz	20.37			
			SAM EMI level				

5 Packaging Information

Table 35 APM32F103x4x6x8xB/APM E 32103xBMARKING

Package Name	Size	Marking of Apex samples
QFN36	6*6*0.9	
QFP48	7*7*1.6	
QFP64	10*10*1.6	
QFP100	14*14*1.6	

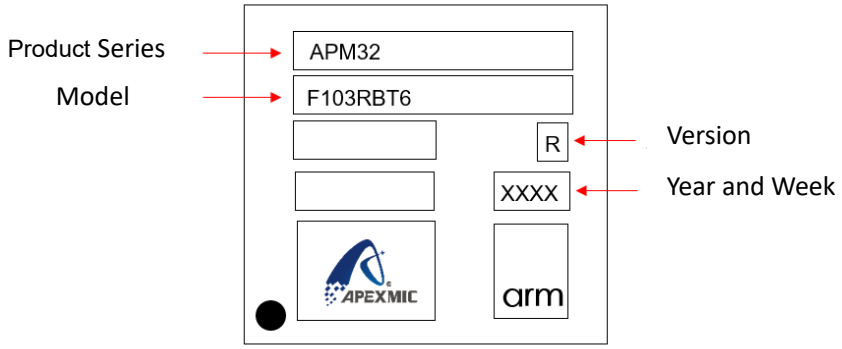
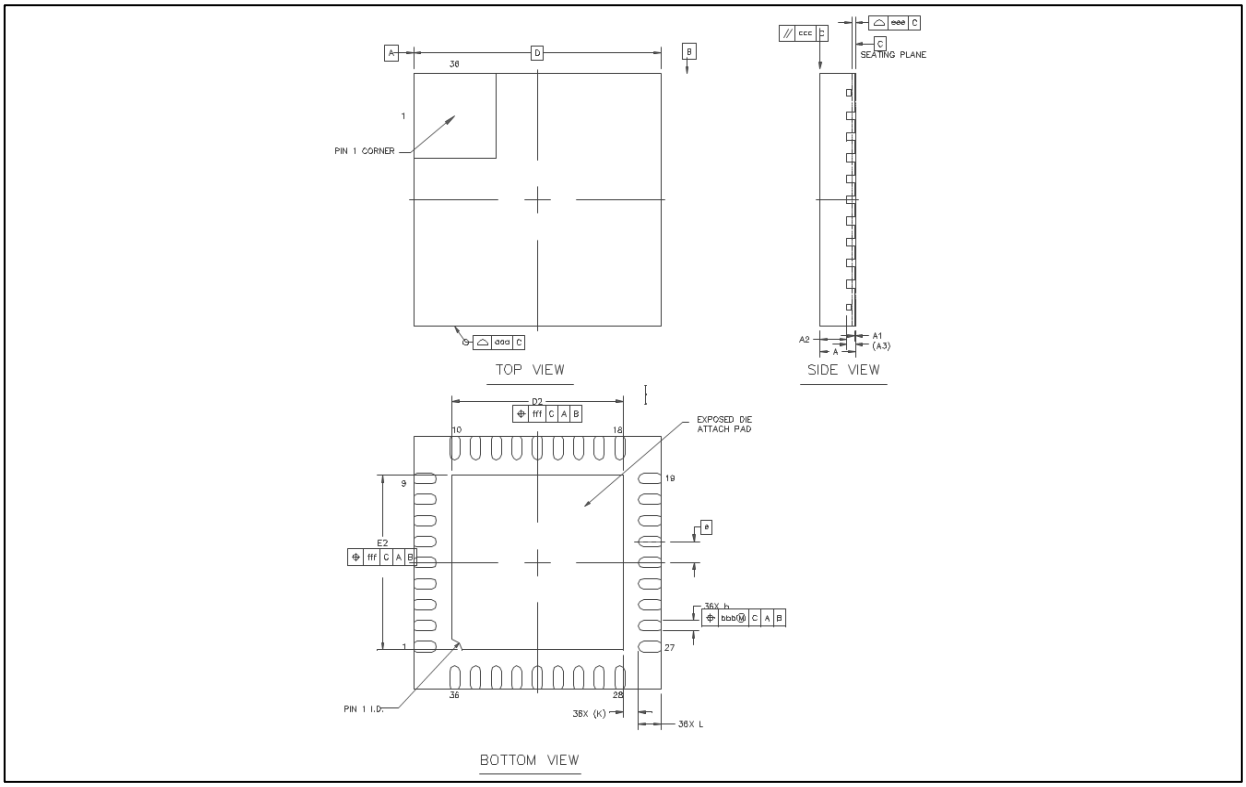


Figure 18　QFN36 Package Diagram



1. Drawing is not to scale.

2. The inside of the pad on the back is not connected to VSS or VDD.

3. There is a pad on the bottom of the QPN package that should be soldered to the PCB.

All pins should be soldered to the PCB.

Table 36 QFN36 Package Data

		SYMBOL	MIN	NOD	MAX
TOTAL THCKNESS		A	0.8	0.85	0.9
STANO OFF		A1	0	0.02	0.05
MOLO THCKNESS		A2	---	0.65	---
L/F THCKNESS		A3	0.203REF		
LEAD WIDTH		b	0.2	0.25	0.3
BOOY SIZE	X	D	6 BSC		
	Y	E	6 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	4.05	4.15	4.25
	Y	E2	4.05	4.15	4.25
LEAD LENGTH		L	0.45	0.55	0.65
LEAD TIP TO EXPOSE PAD EDGE		k	0.375 REF		
PACKAGE EOGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
EXPOSED PAD OFFSET		fff	0.1		

Figure 19　LQFP100 Package Diagram

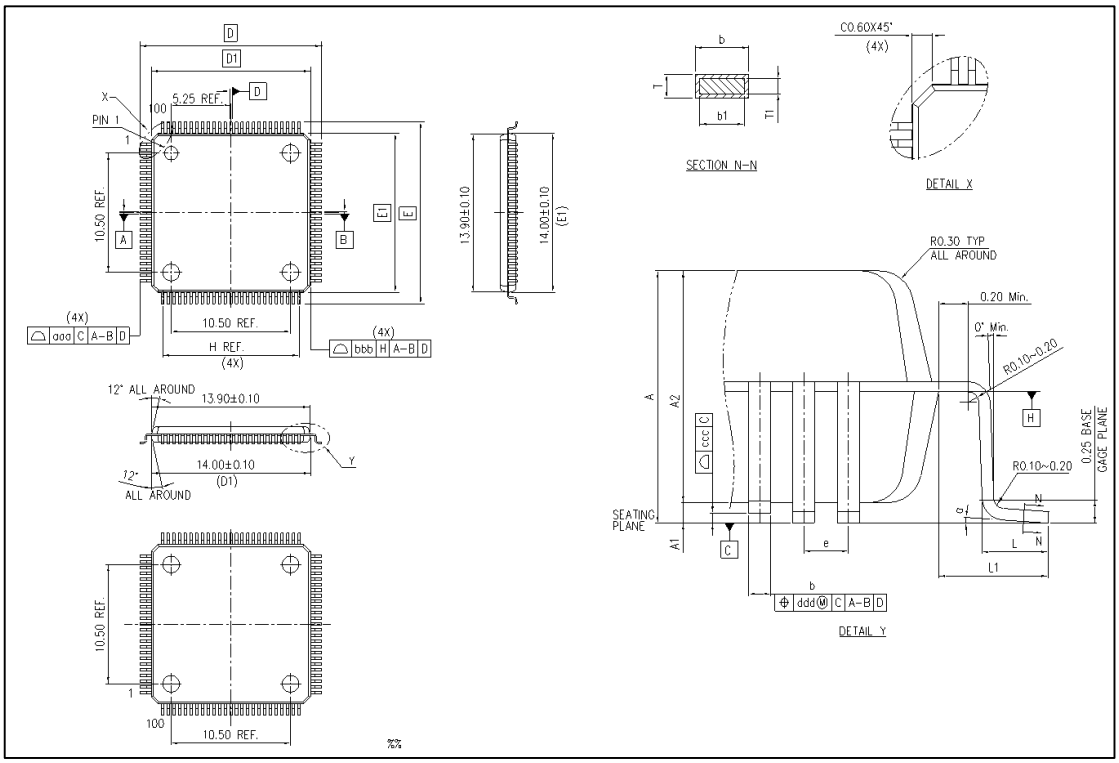


Table 37　LQFP100 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)

S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	16.00±0.20	LEAD TIP TO TIP
5	D1	14.00±0.10	PKG LENGTH
6	E	16.00±0.20	LEAD TIP TO TIP
7	E1	14.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(12.00)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

NOTES	DESCRIPTION		SPECIFICATION
S/N	GENERAL TOLERANCE.	DISTANCE	±0.1
1		ANGLE	±2.5
2	MATTE FINISH ON PACKACE BOOY SURFACE EXPECT EJECTION AND PIN 1 MARKING		Ro0.8~0.2um
3	ALL MOLDED BOOY SHARP CORNE RADLL UNLESS OTHERWISE SPECIFIED		MAX.R0.20
4	PACKAGE/LEADFEAME MISALIGNMENT(X、Y)：		MAX.0.127
5	TOP/BTM PACKAGE MISALIGNMENT(X、Y)：		MAX.0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR META PROTRUSION OR CUTTING BURR		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

Figure 20　LQFP64 Pakcage Diagram

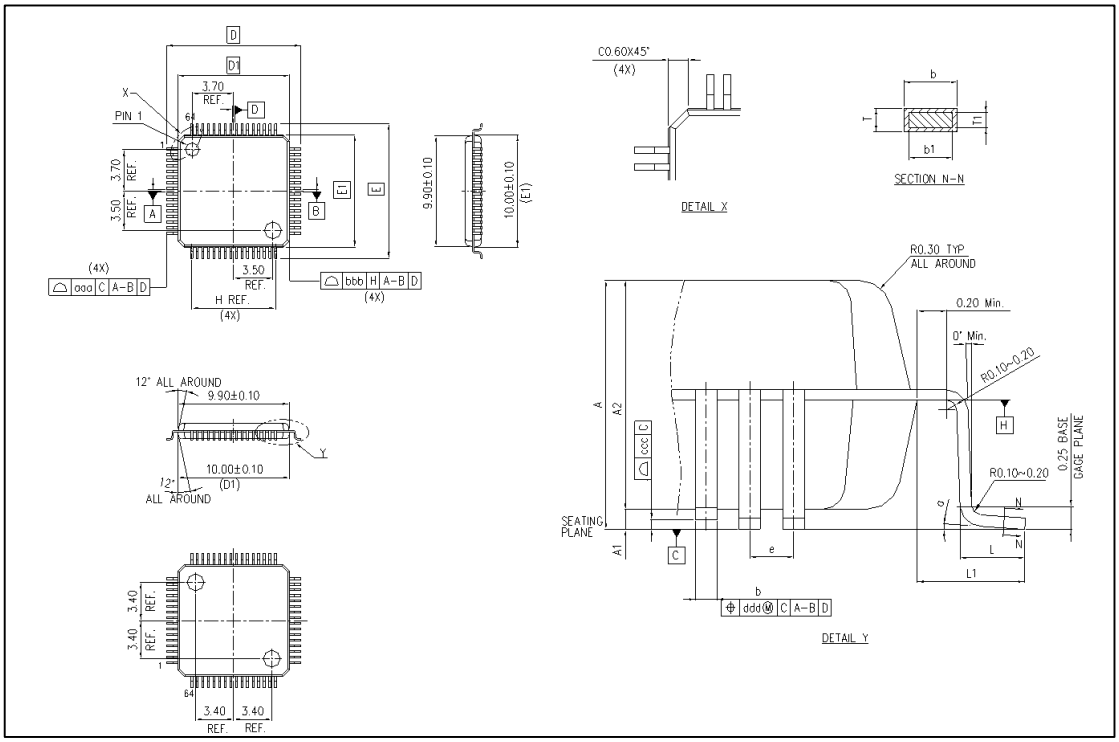


Table 38　LQFP64 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)

S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	0.100±0.050	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	12.000±0.200	LEAD TIP TO TIP
5	D1	10.000±0.100	PKG LENGTH
6	E	12.000±0.200	LEAD TIP TO TIP
7	E1	10.000±0.100	PKG WDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF	LEAD LENGTH
10	T	$0.150^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.220±0.050	LEAD WIDTH
14	b1	0.200±0.030	LEAD BASE METAL WIDTH
15	e	0.500 BASE	LEAD PITCH
16	H(REF.)	(7.500)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

NOTES	DESCRIPTION		SPECIFICATION
S/N	GENERAL TOLERANCE.	DISTANCE	±0.100
1		ANGLE	±2.5
2	MATTE FINISH ON PACKACE BOOY SURFACE EXPECT EJECTION AND PIN 1 MARKING		Ro0.8~0.2um
3	ALL MOLDED BOOY SHARP CORNE RADLL UNLESS OTHERWISE SPECIFIED		MAX.R0.200
4	PACKAGE/LEADFEAME MISALIGNMENT(X、Y)：		MAX.0.127
5	TOP/BTM PACKAGE MISALIGNMENT(X、Y)：		MAX.0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR META PROTRUSION OR CUTTING BURR		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

Figure 21　LQFP48 Package Diagram

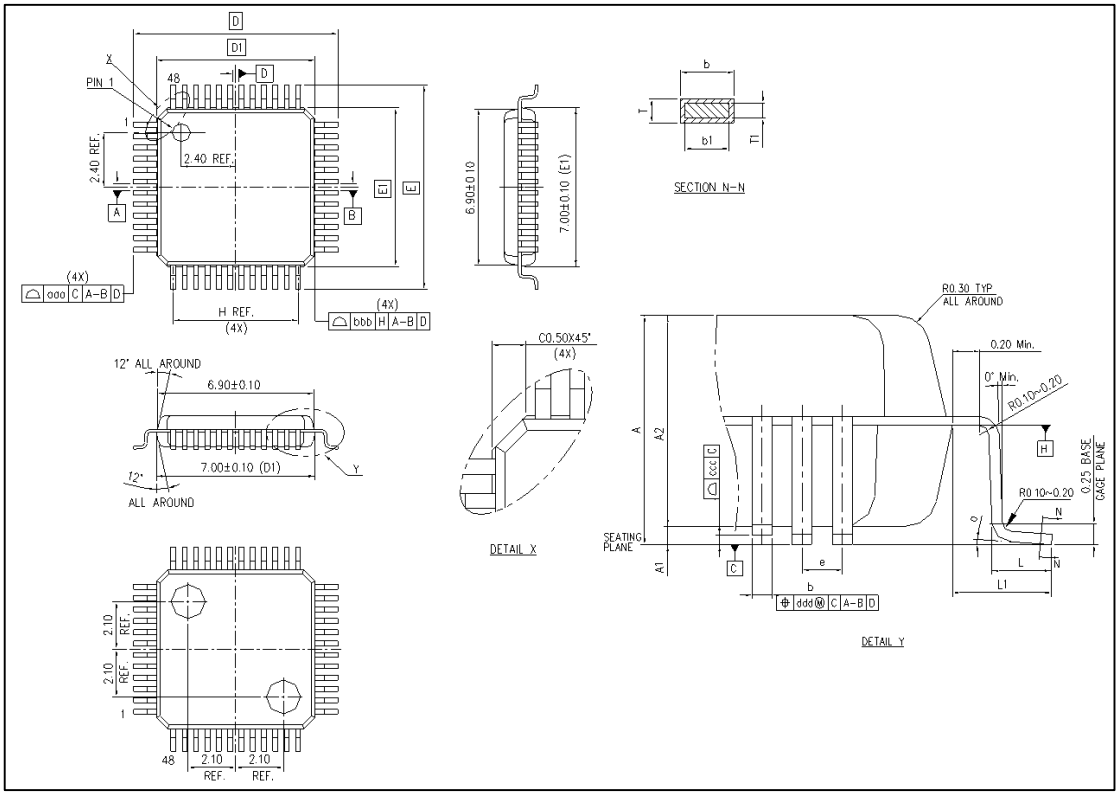


Table 39　LQFP64 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)

S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

NOTES	DESCRIPTION		SPECIFICATION
S/N	GENERAL TOLERANCE.	DISTANCE	±0.10
1		ANGLE	±2.5
2	MATTE FINISH ON PACKACE BOOY SURFACE EXPECT EJECTION AND PIN 1 MARKING		Ro0.8~0.2um
3	ALL MOLDED BOOY SHARP CORNE RADLL UNLESS OTHERWISE SPECIFIED		MAX.R0.20
4	PACKAGE/LEADFEAME MISALIGNMENT(X、Y)：		MAX.0.127
5	TOP/BTM PACKAGE MISALIGNMENT(X、Y)：		MAX.0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR META PROTRUSION OR CUTTING BURR		

7	COMPLIANT TO JEDEC STANDARD: MS-026

6 Ordering Information

Example: APM32 F 103 C 8 T 6 xxx

Device family

APM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose
E = enhanced

Device subfamily

103 = performance line

Pin count

T = 36 pins
C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory

Package

T = LQFP
U= QFN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx= programmed parts
TB = tape and real

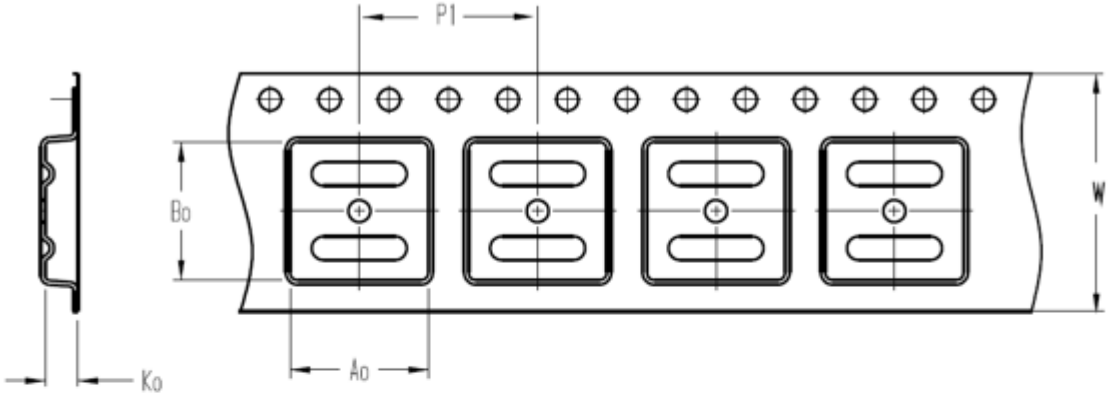
Table 40 Ordering Information Table

Oder No.	FLASH(KB)	SRAM(KB)	Package	Temperature range
APM32E103CBT7	128	20	LQFP48	Industrial level -40°C~105°C
APM32E103RBT7	128	20	LQFP64	Industrial level -40°C~105°C
APM32E103VBT7	128	20	LQFP100	Industrial level -40°C~105°C
APM32F103T4U6	16	6	QFN36	Industrial level -40°C~85°C
APM32F103T6U6	32	10	QFN36	Industrial level -40°C~85°C
APM32F103T8U6	64	20	QFN36	Industrial level -40°C~85°C
APM32F103TBU6	128	20	QFN36	Industrial level -40°C~85°C
APM32F103C4T6	16	6	LQFP48	Industrial level -40°C~85°C
APM32F103C6T6	32	10	LQFP48	Industrial level -40°C~85°C
APM32F103C8T6	64	20	LQFP48	Industrial level -40°C~85°C
APM32F103CBT6	128	20	LQFP48	Industrial level -40°C~85°C
APM32F103R4T6	16	6	LQFP64	Industrial level -40°C~85°C
APM32F103R6T6	32	10	LQFP64	Industrial level -40°C~85°C
APM32F103R8T6	64	20	LQFP64	Industrial level -40°C~85°C
APM32F103RBT6	128	20	LQFP64	Industrial level -40°C~85°C
APM32F103V8T6	64	20	LQFP100	Industrial level -40°C~85°C
APM32F103VBT6	128	20	LQFP100	Industrial level -40°C~85°C
APM32F102C4T6	16	6	LQFP48	Industrial level -40°C~85°C
APM32F102C6T6	32	10	LQFP48	Industrial level -40°C~85°C
APM32F102C8T6	64	20	LQFP48	Industrial level -40°C~85°C
APM32F102CBT6	128	20	LQFP48	Industrial level -40°C~85°C
APM32F102R4T6	16	6	LQFP64	Industrial level -40°C~85°C
APM32F102R6T6	32	10	LQFP64	Industrial level -40°C~85°C
APM32F102R8T6	64	20	LQFP64	Industrial level -40°C~85°C
APM32F102RBT6	128	20	LQFP64	Industrial level -40°C~85°C
APM32F101T4U6	16	6	QFN36	Industrial level -40°C~85°C
APM32F101T6U6	32	10	QFN36	Industrial level -40°C~85°C
APM32F101T8U6	64	20	QFN36	Industrial level -40°C~85°C
APM32F101TBU6	128	20	QFN36	Industrial level -40°C~85°C
APM32F101C4T6	16	6	LQFP48	Industrial level -40°C~85°C
APM32F101C6T6	32	10	LQFP48	Industrial level -40°C~85°C
APM32F101C8T6	64	20	LQFP48	Industrial level -40°C~85°C
APM32F101CBT6	128	20	LQFP48	Industrial level -40°C~85°C
APM32F101R4T6	16	6	LQFP64	Industrial level -40°C~85°C
APM32F101R6T6	32	10	LQFP64	Industrial level -40°C~85°C
APM32F101R8T6	64	20	LQFP64	Industrial level -40°C~85°C
APM32F101RBT6	128	20	LQFP64	Industrial level -40°C~85°C
APM32F101V8T6	64	20	LQFP100	Industrial level -40°C~85°C
APM32F101VBT6	128	20	LQFP100	Industrial level -40°C~85°C

7 Package Information

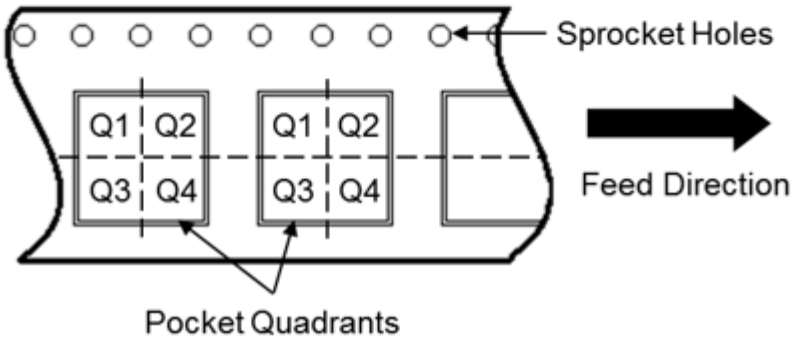
Figure 22 Strip Package Specification Diagram

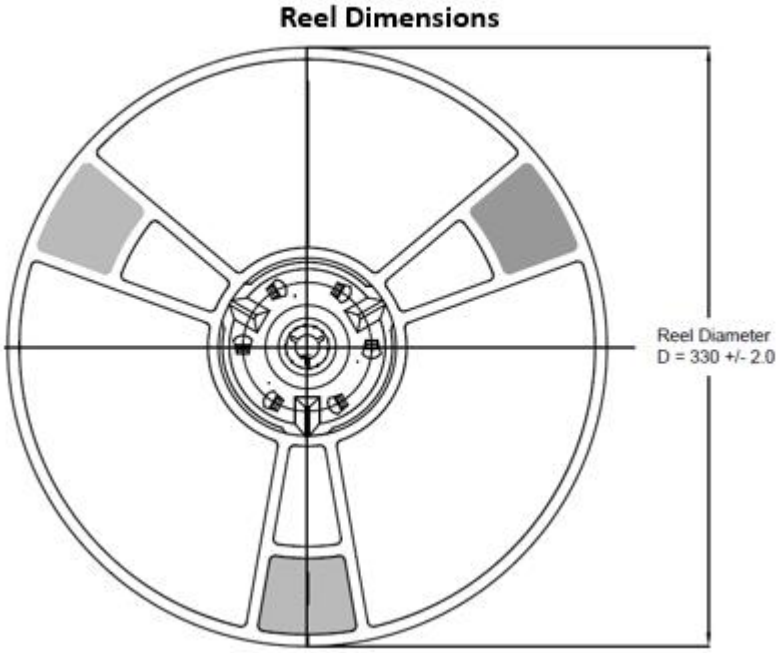
Tape Dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Quadrant Assignments For PIN1 Orientation In Tape





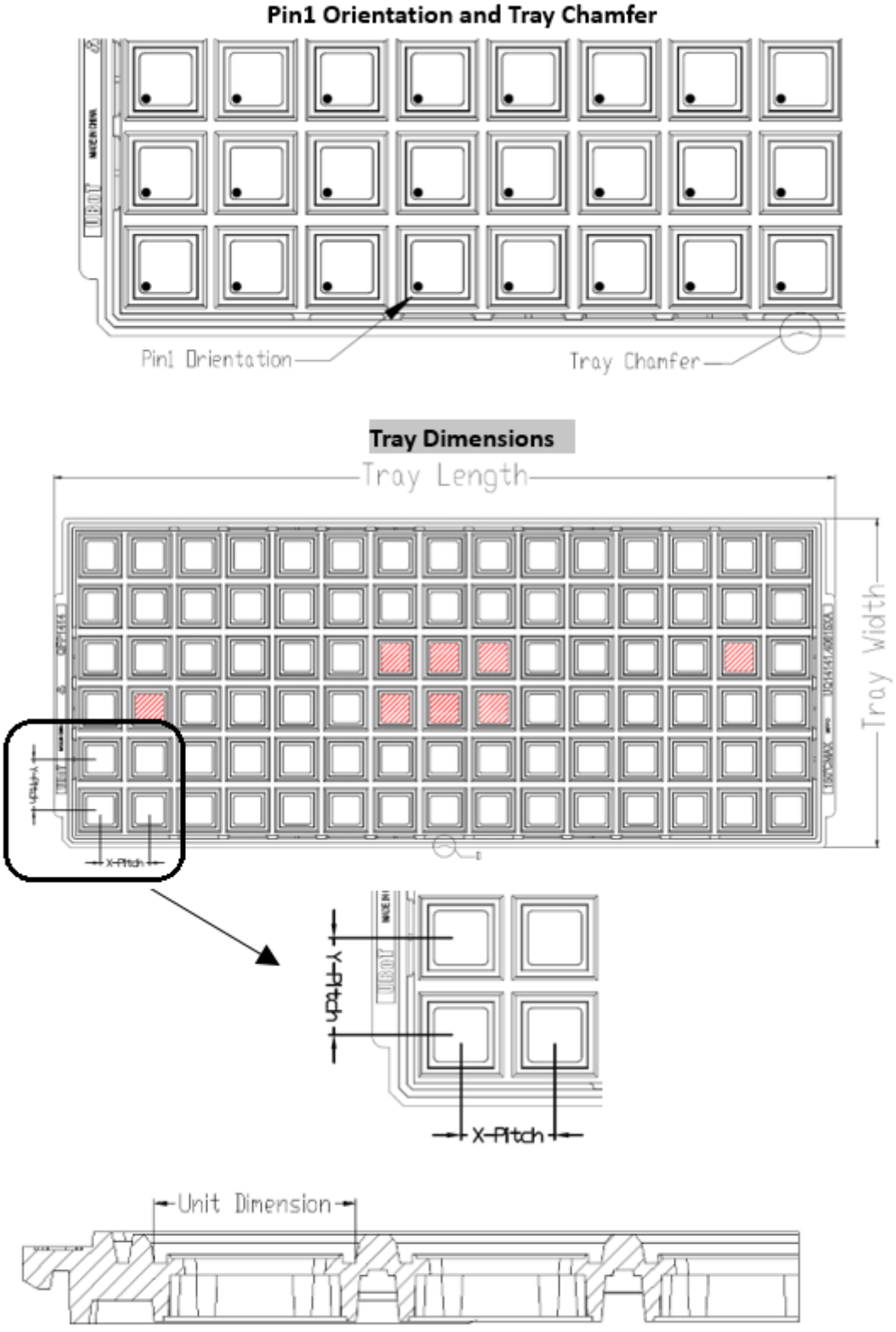
All pictures are only for reference, appearance depends on products

Table 41 Strip Package Parameters Specification

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
APM32E103RBT7	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103RBT6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F102RBT6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F101RBT6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103R8T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F102R8T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F101R8T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103R6T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F102R6T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F101R6T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103R4T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F102R4T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F101R4T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32E103CBT7	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F103CBT6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F102CBT6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F101CBT6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1

APM32F103C8T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F102C8T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F101C8T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F103C6T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F102C6T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F101C6T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F103C4T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F102C4T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F101C4T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F103TBU6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F101TBU6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F103T8U6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F101T8U6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F103T6U6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F101T6U6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F103T4U6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F101T4U6	VFQFPN	36	2500	330	6.4	6.4	1.4	8	16	Q1

Figure 23 Tray Package Diagram



All the pictures are only for reference, appearance depends on products

Table 42 Tray Package Parameters Specification

Device	Package Type	Pins	SPQ	X-Dimension	Y-Dimension	X-Pitch	Y-Pitch	Tray Length	Tray Width
				(mm)	(mm)	(mm)	(mm)	(mm)	(mm)
APM32E103VBT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F103VBT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F101VBT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F103V8T6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F101V8T6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32E103RBT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F102RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F101RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F102R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F101R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103R6T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F102R6T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F101R6T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103R4T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F102R4T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F101R4T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32E103CBT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103CBT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F102CBT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F101CBT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F102C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F101C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103C6T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F102C6T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F101C6T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103C4T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F102C4T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F101C4T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103TBU6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F101TBU6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F103T8U6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F101T8U6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F103T6U6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F101T6U6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F103T4U6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F101T4U6	VFQFPN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9

8 Reversion History

Table 43 Document Reversion History

Date	Version	Changes
2019.2.14	1.0.0	Initial release
2019.2.26	1.0.1	Add the notes in Table 8
2019.5.6	1.0.2	Voltage was changed from 1.8V to 1.6V