1.54 inch E-paper Display

GooDisplay®

GDEM0154F61H

Dalian Good Display Co., Ltd.

Product Specifications

Customer	Standard
Description	ePaper Display
Model Name	GDEM0154F61H
Date	2026/05/15
Revision	1.0

	Design Engineering		
	Approval	Check	Design
			

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1. Over View

GDEM0154F61H is an Active Matrix EPD all-in-one driver with timing controller for ESL.The sources have 2-bit outputs per pixel to support white/black/red/yellow.The 1.50 inch active area contains 200×200 pixels.The module is a TFT-array driving electrophoresis display,with integrated circuits including gate driver,source driver,MCU interface,timing controller,oscillator, DC-DC,SRAM,LUT,VCOM.Module can be used in portable electronic devices,such as Electronic Shelf Label (ESL)System.

2. Features

◆200×200 pixels display
◆High contrast High reflectance
◆Ultra wide viewing angle Ultra low power consumption
◆Pure reflective mode
◆Bi-stable display
◆Commercia temperatur range
◆Landscape portrait modes
◆Hard-coat antiglare display surface
◆Ultra Low current deep sleep mode
◆On chip display RAM
◆Waveform can stored in On-chip OTP or written by MCU
◆Serial peripheral interface available
◆On-chip oscillator
◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
◆I²C signal master interface to read external temperature sensor
◆Built-in temperature sensor

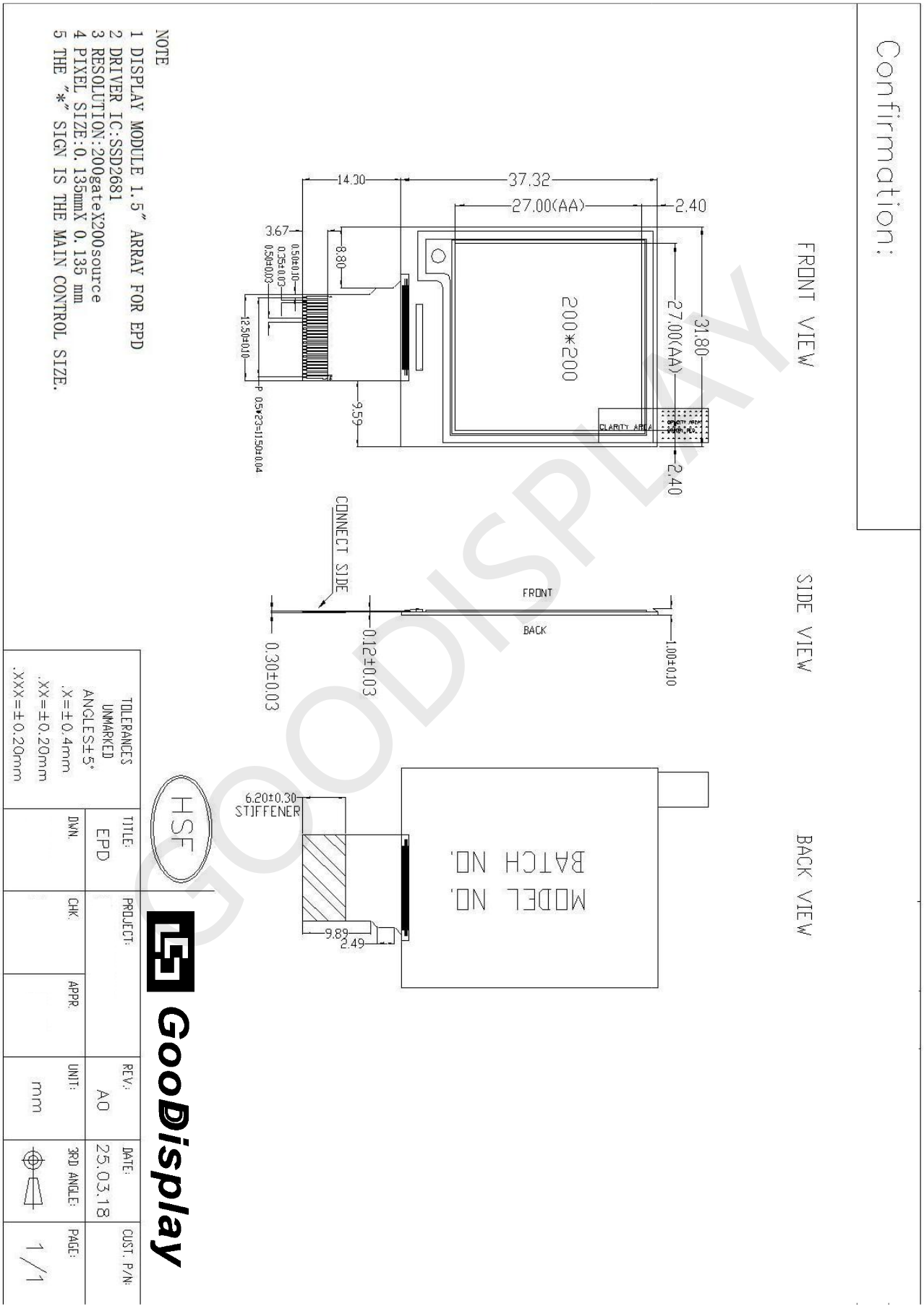
3. Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	1.50	Inch	
Display Resolution	200(H)×200(V)	Pixel	DPI:188
Active Area	27.00×27.00	mm	
Pixel Pitch	0.135×0.135	mm	
Pixel Configuration	Square		
Outline Dimension	31.80(H)×37.32(V)×1.00(D)	mm	
Weight	2.32±0.5	g	

Temperature Range(°C)		0-9	10-19	20-29	30-40	Units
White State	TYP L*	64	63	63	63	
	MIN L*	62	62	62	62	
	a*	≤0	≤0	≤0	≤0	
	b*	≤2.5	≤2.5	≤2.5	≤2.5	
Black State	TYP L*	9	9	9	9	
	MAX L*	11	11	11	11	
	a*	≤9	≤9	≤8	≤10	
Red State	MIN L*	23	23	24	23	
	TYP a*	36	38	40	40	
	MIN a*	34	34	38	38	
	MAX b*	34	34	34	34	
Yellow State	MIN L*	50	50	54	54	
	TYP b*	55	63	66	66	
	MIN b*	53	56	60	60	
	MAX a*	18	18	18	18	
Ghosting		≤2	≤2	≤2	≤2	delta E

Notes: Luminance meter:Eye-One Pro Spectrophotometer.

4. Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep Open
5	VDHR	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	Note 5-6
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	Note 5-6
8	BS	I	Bus Interface selection pin	Note 5-5
9	BUSY_N	O	Busy state output pin	Note 5-4
10	RST_N	I	Reset signal input.Active Low.	Note 5-3
11	DC	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin(SPI)	
14	SDA	I/O	Serial Data pin(SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VDD	
16	VDD	P	Power Supply for the chip	
17	GND	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD.A capacitor should be connected between VDDD and GND	
19	VPP	P	FOR TEST	Keep Open
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I= Input Pin, O = Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C= Capacitor Pin

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin (DC) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent.The chip would put Busy pin Low when

a. Outputting display waveform

b. Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)-8 bits SPI
H	3-lines serial peripheral interface(SPI)-9 bits SPI

Note 5-6:This pin need connect to the VSS if there is no external temperature sensor. External pull up resistor is required when connecting to I2C slave.

6.Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD,VDDIO	-0.5 to+4.0	V
Logic Input voltage	VIN	-0.5 to VDDIO+0.5	V
Logic Output voltage	VOUT	-0.5 to VDDIo+0.5	V
Operating Temp range	TOPR	0 to+40	℃.
Storage Temp range	TSTG	-25 to +70	℃.
Optimal Storage Temp	TST Go	23±3	℃.
Optimal Storage Humidity	HST Go	55±10	%RH

Note:

1.Maximum ratings are those values beyond which damages to the device may occur.Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

2.The display screen should be kept white and face up during storage.Please refer to the [Reliability Test] section.

6.2 Panel DC Characteristics

The following specifications apply for:GND=0V,VDD=3.0V,TOPR=23℃.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	GND	-		-	0	-	V
Logic supply voltage	V_{DD}	-	VDD	2.2	3.0	3.6	V
Power for interface logic pins	V_{DDIO}	-	VDDIO	2.2	-	3.6	V
Core logic voltage	V_{DDD}		VDDD	-	-	-	V
VCOM_DC output voltage	V_{COM}		VCOM	-3.0		-0.2	
High level input voltage	V_{IH}	-	-	0.8 V_{DDIO}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{DDIO}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.8 V_{DDIO}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.2 V_{DDIO}	V
Typical power	P_{TYP}	V_{DD} =3.0V	-	-	4.8	-	mW
Deep sleep mode	P_{STPY}	V_{DD} =3.0V	-	-	0.0012	-	mW
Typical operating current	Iopr_VDD	V_{DD} =3.0V	-	-	1.6	- -	mA
Full/Fast Image update	-	23 ℃	-	-	20/12	-	sec
Deep sleep mode current	$Idslp_{VDD}$	DC/DC off No clock No input load Ram data not retain	-	-	0.4	TBD	uA

Notes: 1. The typical power measurement method is as follows, and the output is reported according to the test screen provided by the.

2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by.

4.Electrical measurement:Tektronix oscilloscope-MS044, Tektronix current probe-TCPA300.

6.3 MCU Interface

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1.Different MCU mode can be set by hardware selection on BS pins.The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	DC	RST_N
BS1=L 4-wire SPI	SDA	SCL	CSB	DC	RST_N
BS1=H 3-wire SPI	SDA	SCL	CSB	L	RST_N

Table 6-3-1:MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface(4-wire SPI)

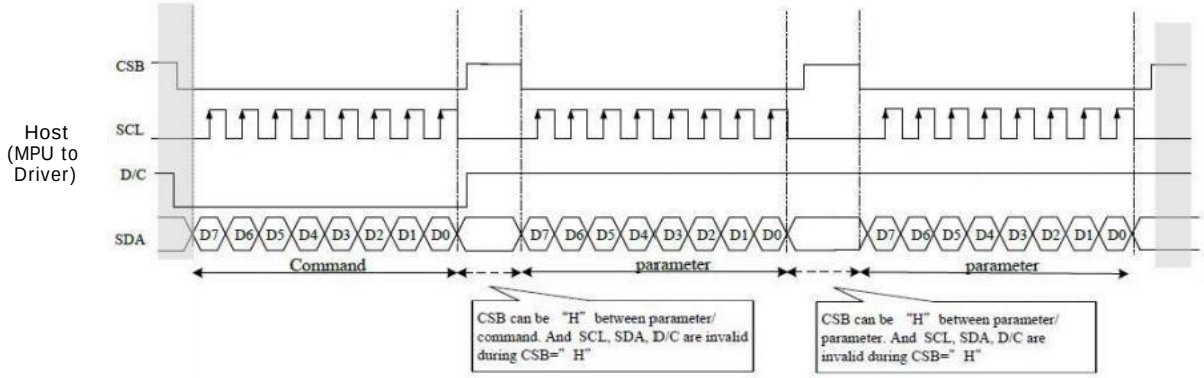
The serial interface consists of serial clock SCL,serial data SDA,DC,CSB.This interface supports Write mode and Read mode.

Function	CSB	DC	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 6-3-2:Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1:4-wire SPI mode



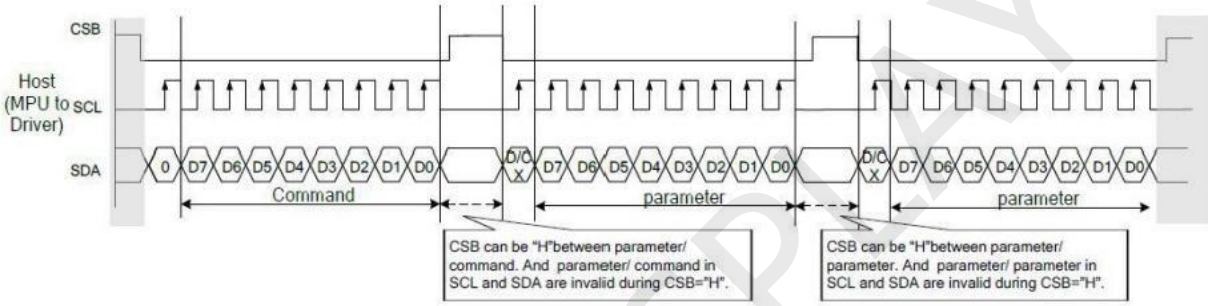
6.3.3 MCU Serial Interface (3-wire SPI)

Function	CSB	DC	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

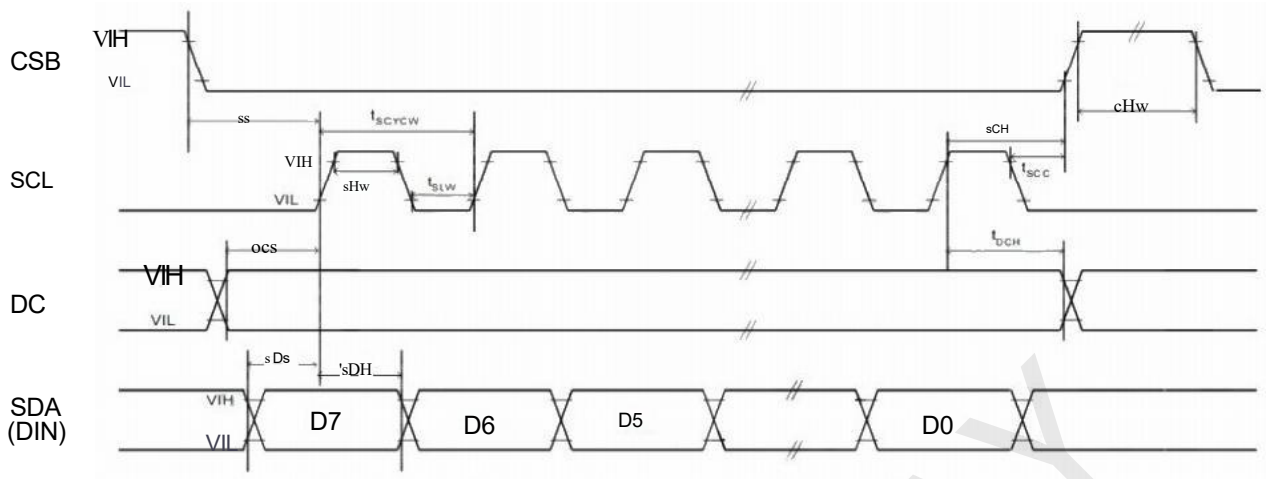
Table 6-3-3:Control pins of 3-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

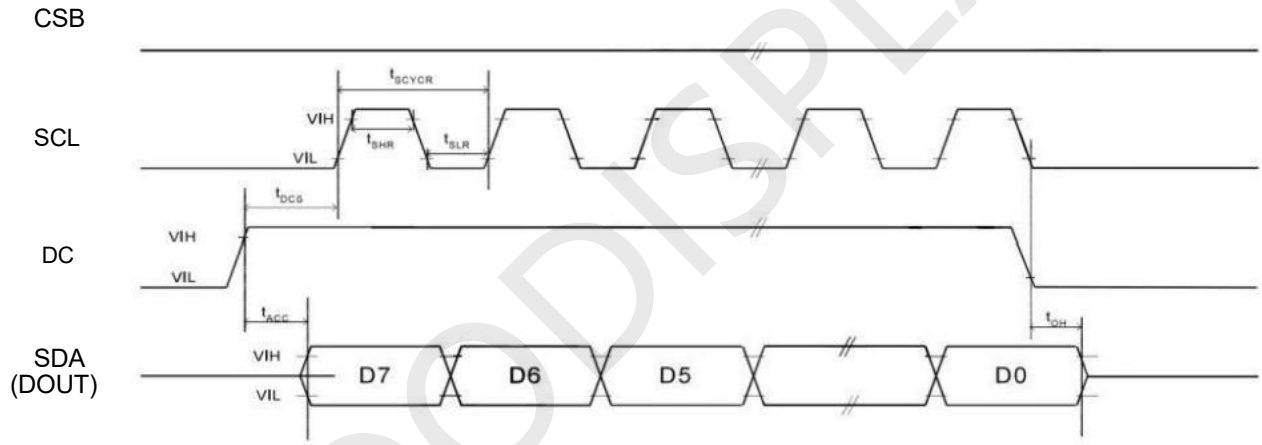
Figure 6-3-2:3-wire SPI mode



6.3.4 Interface Timing



4-wire SPI characteristics(write mode)



4-wire SPI characteristics(read mode)

Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
tcss	CSB select setup time	TBD			ns
tscH	CSB select hold time	TBD			ns
tsoc	CSB deselect setup time	TBD			ns
taw	CSB deselect hold time	TBD			ns
tsCYCw	Serial clock cycle(Wnte)	TBD			ns
tsw	SCL"H"pulse width(Write)	TBD			ns
tsw	SCL"L"pulse width(Write)	TBD			ns
tscYa	Serial clock cycle (Read)	TBD			ns
tsR	SCL"H"pulse width(Read)	TBD			ns
tsLR	SCL"L"pulse width(Read)	TBD			ns
tsos	Data setup time	TBD			ns
tsDH	Data hold time	TBD			ns
tocs	DC setup time	TBD			ns
tocH	DC hold time	TBD			ns
tAcc	Access time			TBD	ns
toH	Output disable time	TBD			ns

Note:All timings are based on 20%to 80%of VDDIO-GND

7.Command Table

R	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0]=2Fh [POR] B7:0j=09h [PORj
0	1		Az	As	As	0	A3	A2	A1	Ao		A[7:6]~RES[1:0] Display Resolution setting(source x gate) 00b:200×200(Default) 01b:152×152 10b:104 x104 11b:160 ×160 "**Remark:** **Inactive** Gate outputs wil be VGL for DRF and AMV. **Inactive** Source outputs will follow VCOM LUT output for DRF A[5]-B_mode Blanking Mode for voltage switching,the duration setting follow CDI. 0:Mode A Blanking time only for ACVCOM. 1:Mode B(Default) Blanking time for ACVCOM or switch mode of source power. A[3]~UD Gate Scan **Direction:** 0:Scan **down.** First line **to Last line:**Gn-1...G0 1:Scan up.**(Default)** First line to Last line:G0...Gn-1 A[2]~SHL Source Shift Direction: 0:Shift left. First data to Last data:Sn-1...S0 1:Shift nght.(Default) First data to Last data:S0...Sn-1 A[1]-SHD_N Booster Switch: 0:Booster off,register data are kept,and Source/VBD/ Vcom are kept OV or floating. 1:Booster on.(Default) A[O]-

												RST_N Soft Reset: 0:The controller is reset.Reset all registers to their defaut value.Driver allfunction will be disabled. 1:Normal operation(Default). BUSY_Nwill output low during operation.
0	1		B7	Be	Bs	Ba	B3	B2	B1	Bo		B[7]~LUT_EN

RM#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												0.During reset,auto load LUTfrom MTP ifit is valid. When PON/DRF,analog setting will follow the content of MTP. (Default) 1:During reset,no action to load LUT from MTP.When PON/DRF,analog setting will folow the content of MCU B[6:5]-FOPT[1:0] FOPTfundion oob:NO effect.Scan 1 frame after waveform finished (Default) 01b:Wil scan 1 frame same as last output (of LUT)after waveform finished. 10b:**Wilscan** 1 frame with Floating output after waveform **finished.** 11b:No Scan after waveform finished(Power offfloating) B4]~VCMZ vCOM Hi-Z option 0.NO effect. (default) 1:VCOM is always floating. B[3]~TS_AUTO Temperature Sensor auto option 0.NO effect. 1:Before loading MTP,Temperature Sensor will be activated automatically one time. (defauf) B[2]~TIEG VGLpowe**r off option** 0.NO **effect. (default)** 1:After **power offboo**ster,VGL wil be tied to GND. B[1]-NORG vCOM display end GND oplion **0:NO effect**. (default) **1:After refr**eshing display,VCOM is tied to GNDbefore **power off** B[Q]~VC_LUTZ **VCOM** display end floating option **0.NO** effect. 1:After refreshing display,the output of VCOM is set to floating automatically(default)

RME	DIC#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	PWR	Power setting Register A[5:0]=07h [PORI B[7:0j=FOh [PORj C[6:0]=00h [POR] D[6:0j=00h [PORj E[6:0]=00h jPOR F[6:0j=00h jPORj
0	1		0	0	0	0	0	A2	Ar	Ao		A[2]~VSC_EN Source LVpower selection: 0.External source power for VSH2 pin. 1:Intemal DCDCfunction for generate source power. (default) A[1]~VS_EN Source LVpower selection: 0.External source power for VSH1 and VSL pin. 1:Internal DCDC function for generate source power. (default) A[0]~VG_EN Gate power selection: 0.External gate power for VGH and VGL pin. 1:Internal DCDC function for generate gate power. (default)
0	1		1	1	1	1	0	0	B:	Bo		B[1:0]-VGPN[1:0] Internal VGH/VGLVoltage LevelSelection: VGPN [1:0] Gate Voltage Level 00 VGH=20V,VGL=20V(Default) VSH=15V.VSL=-15V 01 VGH=17V,VGL=-17V VSH=15V,VSL=-15V 10 VGH=15V,VGL=15V VSH=13V,VSL=-13V 11 Reserved.
0	1		0	C	Cs	C	Cs	C_2	C+	Co		C6:0]-VSPL[6:0 Internal Source Voltage Level Selection for VSH2@Mode0 VSPL[6:01 Voltage Level 00h 3.0V(defaut) 02h 3.2V 04h 3.4V 06h 3.6V 76h 14.8V 78h 15.0V Other Reserved
0	1		0	D	Ds	D4	D_3	D_2	D_1	Do		D[6:0]~VSNL[6:0] internal Source Voltage Level Selection for VSL@Mode1: VSNL6:0] Voltage Level 00h -3.0V(defaut) 02h -3.2V 04h -3.4V 06h -3.6V : : 76h -14.8V 78h -15.0V Other Reserved

<table>
<tr><th>RM#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>E6</td><td>Es</td><td>E4</td><td>E3</td><td>E2</td><td>E1</td><td>Eo</td><td></td><td>E[6:0]~VSPL2[6:0]
Internal Source Voltage Level Selection for VSH1@Mode1:
VSPL2[6:0] | Voltage Level
00h | 3.0V(default)
02h | 3.2V
04h | 3.4V
06h | 3.6V
: | *
76h | 14.8V
78h | 15.0V
Other | Reserved</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>F6</td><td>Fs</td><td>F4</td><td>F3</td><td>F2</td><td>F1</td><td>Fo</td><td></td><td>F[6:0]~VSNL2[6:0]
Internal Source Voltage Level Selection for VSH2@Mode1:
VSNL2[6:0] | Voltage Level
00h | 3.0V(default)
02h | 3.2V
04h | 3.4V
06h | 3.6V
: | :
76h | 14.8V
78h | 15.0V
Other | Reserved</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>02</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>POF</td><td>Power OFF Command Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>After power off command, driver will power off based on the Power OFF Sequence.
BUSY_N will output low during operation.
The Power OFF command will turn off DCDC, source driver, gate driver, VCOM dniver, temperature sensor, but register and SRAM data will keep untilVDD off.
SD output will base on previous condition.
"Remark POF works at PON only</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>POFS</td><td>Power on/off Sequence Setting Register
A[7:0]=00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>As</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>Ao</td><td></td><td>A[5:4]~T_VDPG_OFF[1:0]
Power off delay from VGL toVGH
00b:20ms(default)
01b:40ms
10b:60ms
11b:80ms

A[1:0]~T_VDS_OFF[1:0]
Power off delay from VSHXNSLtoVGH
00b:20ms(default)
01b:40ms
10b:60ms
11b:80ms</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>PON</td><td>Power ON Command Register
After the Power ON command, driver will power on based on the Power ON Sequence.
BUSY_N will output low during operation.

Remark:
PONInclude booster on, VSHx/VSLx regulator on
With default BTST, timing is >80ms</td></tr>
<tr><td colspan="13"></td></tr>
</table>

RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register(for VGH) A[6:0]=0Fh [POR] B[6:0j=8Bh [PORj cj6:0] =9Ch [PORj Di6:0j=96h [PORj
0	1		0	Aa	As	A4	A3	A2	A:	Ao		A6:4]~VGHSSC_ONT [2:0] VGH booster maximum MOSFET ON time (reserved) A[6:4]=000(Default) A3:2]-T_VGHSSA [1:0]=11(Default) VGH booster soft start Phase A duration A[1:0]~T_VGHSSB [1:0]=11(Defauit) VGHbooster soft start Phase B duration
0	1		1	B_6	B_5	B4	B_3	B_2	B_1	Bo		
0	1		1	C	Cs	C4	Cs	C_2	C1	Co		
0	1		1	Ds	Ds	D4	Ds	D_2	D:	Do		

	Soft Start Phase Peniod (ms)
00	10
01	20
10	
11	40

B6:4]~VGHSSA_DRV[2:0],=000(Defaul)
VGH Phase ADriving Strength
C[6:4]-VGHSSB_DRV[2:0],=001(Default)
VGHPhase BDriving Strength
D[6:4]~VGHSSC_**DRV**[2:0]=001(Defaut)
VGHPhase C Driving Strength

Driving Strength			
000	0	100	(reserved)
001	1	101	(reserved)
010	2	110	(reserved)
011	3(strongest)	111	(reserved)

B[3:0]-VGHSSA_OFFT[[3:0].=1011(Default)
VGH Phase AMinimum OFF Time
C[3:0]-VGHSSB_OFFT[[3:0],=1100(Default)
VGHPhase B Minimum OFF Time
D[3:0]-VGHSSC_OFFT[[3:0].=0110(Defaut)
VGH Phase C MnimumOFF Time

Minimum OFF Time(setting)			
0000	OFFH0	1000	OFFH8
0001	OFFH1	1001	OFFH9
0010	OFFH2	1010	OFFHA
0011	OFFH3	1011	OFFHB
0100	OFFH4	1100	OFFHC
0101	OFFH5	1101	OFFHD
0110	OFFH6	1110	OFFHE
0111	OFFH7	1111	OFFHF

0	0	07	0	0	0	0	0	1	1	1	DSLP	Deep Sleep Register
0	1		1	0	1	0	0	1	0	1		This command makes the chip enter the deep-sleep mode.The deep sleep mode could retun to stand-by mode by hardware reset assertion. The only one parameter is a check code,the command would be executed if check code is A5h.

R#	D/Ca	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	DTM	Data Start transmission Register
0	1		2 bit per pixel KPixel1 [1:0]		KPixel2 [1:0]		KPibe3 [1:0]		KPixel4 [1:0]			This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (2H). Then the chip will startto send data/VCOM for panel. KPixel[1:0] Source Driver Output
卡												
0	1		KPixel (4M-3) [1:0]		KPixel (4M-2) [1:0]		KPibxel (4M-1) [1:0]		KPixel (4M) [1:0]			

	DDX=1 (Default)	DDX=0
00b	Gray 0	Gray 3
01	Gray 1	Gray 2
106	Gray 2	Gray 1
11b	Gray 3	Gray 0

After issue this command, the host must send at least 1-byte data to the device.

0	0	12	0	0	0	1	0	0	1	0	DRF	Display Refresh Command Register
0	1		0	0	0	0	0	0	0	0		After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. BUSY_N will output lowduring operation.
0	0	17	0	0	0	1	0	1		1	AUTO	Auto Sequence Register
0	1		Ay	Ao	As	A4	As	A_2	A_1	Ao		This command makes the chip enter the auto sequence Single-chip application ONLY. Auto Sequence Option 0xA5: Start Auto Sequence (PON>DRF>POF) 0xA7: Start Auto Sequence (PON>DRF>POF>DSLP). Others: No effect BUSY_N will output low during operation.
0	0	30	0	0	1	1	0	0	0	0	PLL	Frame Rate Control register The command controls the dock frequency. A[2:0]=2h [POR]
0	1		0	0	0	0	As	A2	Ai	A		A[3]~Dyna Dynamic Frame Rate 0: Disable (Default) 1: Enable A[2:0]~FR[2:0] lt supports the following frame rates. Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.

FR[2:0]	Frame Rate Selection
000	12.5Hz
001	25Hz
010	50Hz (Default)
011	65Hz
100	75Hz
101	85Hz
110	100Hz
111	120Hz

RN#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register
1	1		Az	As	As	A4	A3	A2	A:	Ao		This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A7:01-TS [7:0]

TS[7:0]	Return Value(degc)
E7h	-25
…	
FFh	-1
00h	0
01h	1
19h	25
…	
31h	49
32h	50

0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register This command selects Temperature offset A7:0]=00h [PORI
0	1		0	0	0	0	As	A2	At	Ao		A3:0]~T03:1]. Temperature offset:

T03:1]	Calculation	T03:1]	Calculation
000	+0	100	-4
001	+1	101	-3
010	+2	110	-2
011	+3	111	-1

0	0	50	0	1	0	1	0	0	0	0	CDI	vCOM and DATA interval setting Register This command indicates the Border Output Selection and the intervalbetween Vcom and data output A7:0]=97h [POR]
0	1		A7	As	As	Aa	As	A2	A:	Ao		A7:5-VBD [2:0] Border Output Selection:

	DDX=1	DDX=0
VBD[201	LUT(Default)	LUT
000	Gray 0	HIZ
001	Gray 1	Gray 3
010	Gray 2	Gray 2
011	Gray 3	Gray1
100	HIZDefaull)	Gray 0

A 4:DDX
Data Polarity for Pbxel Data(See DTM command)
0. Invert
1:Non-invert(Default)
A[3:0~CDI[3:0]
Gate and source blanking time(No gate source scanning)

CDI [3:01	Interval(ms)	CDI [3:0]	Interval(ms)
Oh	2	8h	40
1h	4	9h	60
2h	8	Ah	80
3h	12	Bh	100
4h	14	Ch	120
5h	16	Dh	140
6h	18	Eh	160
7h	20(Default)	Fh	Reserved

User needs to review CDI setting to have stable VCOMin applicafion

RIW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	51	0	1	0	1	0	0	0	1	LPD	Lower Power Detection Register
1	1		0	0	0	0	0	0	0	Ao		BUSY_N will output lowduring operation. Then the LPD status can be read. A[0]~LPD status 0.Low power input VDD<2.5V,seleded by LVD_SEL[1:0]in command LVSEL 1:Normal(default)
0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register A[7:0]=C8h [POR] B7:0]=C8h [POR
0	1		0	0	0	0	0	0	0	0		This command defines alternative resolution A[7:0]~HRES[7:0] Horizontal Display Resolution Remark:Horizontal resolution shoukd be4-mutiple. B[7:0]~VRES[7:0] Vertical Display Resolution eg.HRES=C8h,VRES=C8h UD.SHL Source and gate sequence 00 S199.G199 to S0.G0 01 S0.G199 to S199.G0 10 S199,G0 to S0,G199 11 S0,G0 to S199.G199 Remark: 1)Both PSR.RES&TRES command can set panel resolution.Priority will be givento the last received PSR or TRES command. 2 VRES[7:0]>=79
0	1		Az	A_6	As	A_4	A	A_2	A	Ao		
0	1		0	0	0	0	0	0	0	0		
0	1		B_7	B_6	Bs	B4	B_3	B_2	B_1	Bo		
0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register. A7:0]=00h [POR] B[7:0]=00h [POR]
0	1		0	0	0	0	0	0	0	0		A7:0]~S_start[7:0] First valid source output channel setting Frst valid source output S_start [7:0] | 04h | $S_4$0 (Default) 08h S8 C0h S192 C4h S196 Other Reserved
0	1		Az	A_6	As	A4	As	A_2	A	Ao		
0	1		0	0	0	0	0	0	0	0		
0	1		B7	B6	B5	B4	B3	B2	B1	Bo		B[7:0]~G_start[7:0] First valid gate output channel setting GSST and TRES can define the display window from target source and gate start and end line. GD:First Gactive=G16.G_start[7:0]=16. Last G active=G175,VRES[7:0]=160. SD:First S active=S8.S_start7:0]=8. LastSactive=S119,HRES[7:0]=112. Remark: 1)PSR.RES[1:0]=00 2)G start+VRES<200,S start+HRES<200.

RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0]=48h [POR] B[7:0]=01h [POR] ICi7:0j=01h [PORj
1	1		A	A	As	A	A_3	A_2	A_1	Ao		
1	1		B7	Bs	Bs	B4	B3	B2	B1	Bo		
1	1		Cr	C	Cs	C4	C_3	C_2	C_1	Co		
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A7:0]=00h [PORI
0	1		Az	Ao	As	A	A3	A2	0	Ao		A[7:6~P[1:0] Number of sensing Points 00:2(**Default)** 01:4 10:8 11:1**6** A[5:4]~AMVT[1:0] **Auto** Measure Vcom Time: Sensing Time **00**:5sec. (Default) 01:10 sec. 10:15 sec. 11:20 sec. A[3]~AMVX VCOM measure**ment Gate** settings 0.Gate scan normally during VCOM measurement (Default) 1:AI Ga**tes ON duning** VCOM measurement A[2]~**AMVS** Source output of AMV: 0.Set Source output to OV during Auto Measure VCOM period. (Default) 1:Set Source output to VSH_LV during Auto Measure vCOM period. AO]~AMVE Auto Measure Vcom Enable (/Disable): 0.:Disabled (Default) 1:Enabled BUSYN willoutput low during operation Requirement.AMVworks atPON only
0	0	81	1	0	Q	0	0	0	0	1	w	Auto Measurement VCOM Register This command gets the Vcom value after AMV.
1	1		1	0	As	AA	A_3	A_2	A	Ao		A[5:0]~V5:0]: Vcom read Value,vald range from-0.2Vto-3.0V. W5:01 00h Vcom read value Reserved 04h -0.2V 08h -0.4V 0Ch -0.6V 10h -0.8V 3Ch -3.0V others Reserved

RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0]=00h [POR]
0	1		Az	A_6	As	A4	As	Az	0	0		A7]~MTP_VCM Vcom follow VDCS after RESET. 0:Disable(Default),auto load fromMTP if it is valid. 1:Enable,VCOM value from the VDCS[6:0] A6:0]~VDCS[6:0] VCOM_DC Setting.0.2V step from-0.2V to-3V. VDCS [6:01 VCOM DC Setting 00h Reserved 04h -0.2V 08h -0.4V 0Ch -0.6V 10h -0.8V 3Ch -3.0V others Reserved
0	0	83	1	0	0	0	0	0	1	1	PTLW	PARTIAL WINDOW This command sets partial window address. A[7:0] =00h [POR] B[7:0]=C7h PORI Ci7:0j= 00h [PORj D7:0]=C7h [POR] E7:0 j=00h [PORj
0	1		0	0	0	0	0	0	0	0		A7:0]~HRST[7:0] Horizontal start address B[7:0]~HRED[7:0] Horizontal end address C7:0]-VRST [7:0] Vertical start address D7:0]-VRED[7:0] Vertical end address E[0]～PMODE 0.disable partial mode(Default) 1:enable partialmode Gate scan bothinside and outside of the partial window Note: 1 HRST[7:0]<=HRED[7:0] 2)VRST[7:0]<=VRED [7:0]
0	1		A7	As	As	At	As	A2	Ai	Ao		
0	1		0	0	0	0	0	0	0	0		
0	1		B7	Be	Bs	BA	B_3	B2	B	Bo		
0	1		0	0	0	0	0	0	0	0		
0	1		C_7	Co	Cs	C4	C_3	C_2	C_1	Co		
0	1		0	0	0	0	0	0	0	0		
0	1		D_7	D_6	D_5	Da	Da	D_2	D:	Do		
0	1		0	0	0	0	0	0	0	Eo		
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set MTP program mode After this command is issued,the chip wouldenter the program mode. After the programming procedure completed,a hardware reset is necessary for leave the program mode BUSY_N will output lowunti PGM mode is ready.
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to exeaute MTP program After this command is issued,the chip would program the MTP. BUSY_N will output lowduring operation. Requrement InPON mode with internal programming power.

RW#	D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command Description	
0	0	92		0	0	1	0	0	1	0	RMTP	Read MTP Data
1	1		1t~dummy 2nd~N+1th Parameter									This command is to read the MTP content from SRAM. The 1 byte read is dummy byte. The 2byte read is the content of Address 0in MTP The N+1#byte read is the content of Address nin MTP After issue this command, the host must read at least 1 byte data from the device.
0	0	EO	1	1	1	0	0	0	0	0	cCSET	CCSET **for tem**perature input selection A[7:0]=00h [POR]
0	1		0	0	0	0	0	0	Ai	0		A[1]=TSFIX Temperature Input selection 0:Use Intermal Temperature sensor(Default) 1:Use TSSET[7:0]value
0	0	E3	1	1	1	0	0	0	1	1	PwS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refreshperiod. A[7:0]=65h [POR]
0	1		A_7	Ag	As	A4	A_3	A_2	A	Ao		If the output voltage ofVCOMSource is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. A7:4]=VCOM_W[3:0

VCOM_W [3:0]	_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)
0	Reserved	8	8
1	1	9	9
2	2	10	10
3	3	11	11
4	4	12	12
5	5	13	13
6	6 [Default]	14	14
7	7	15	15

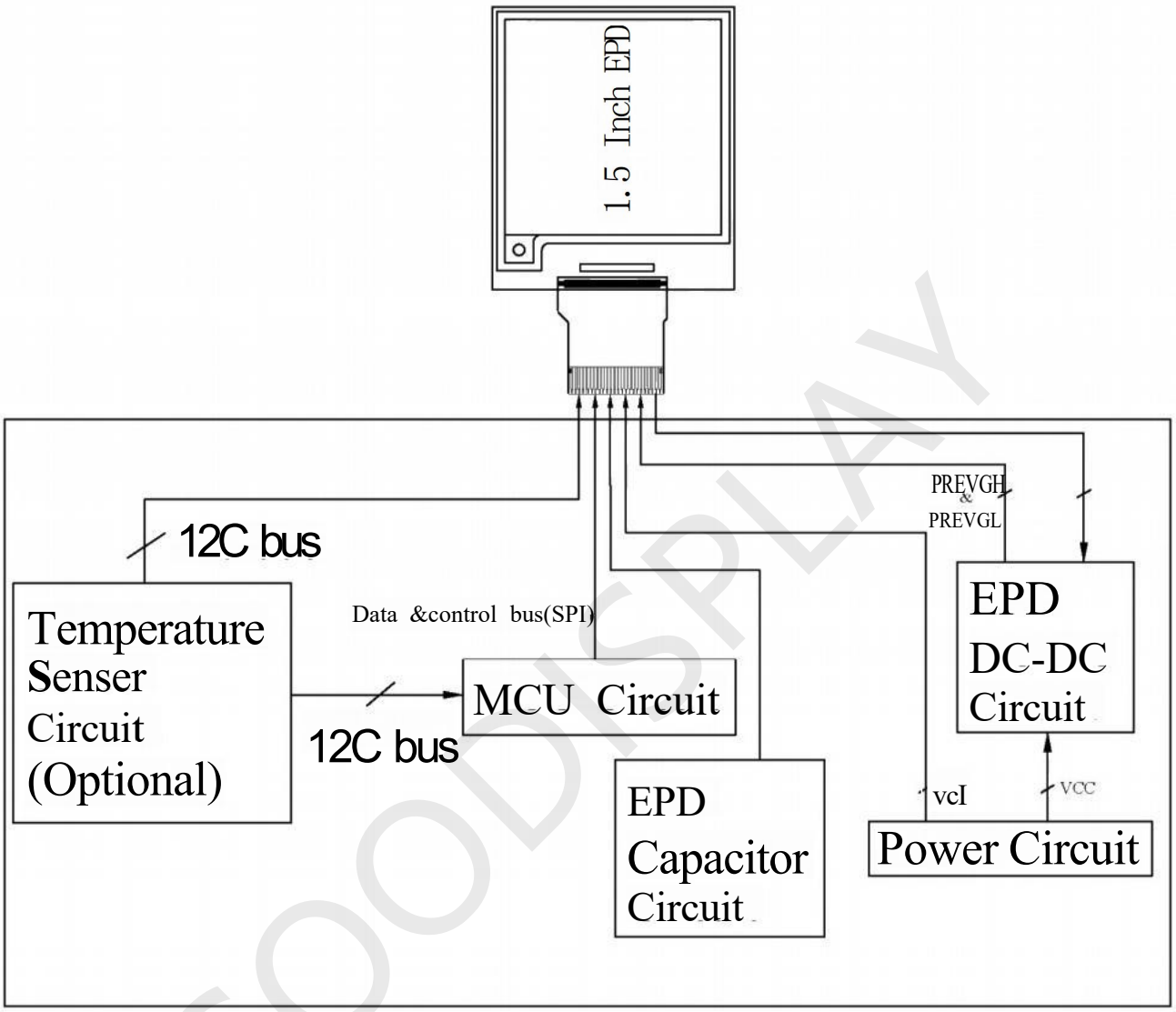
A|3:0]=SD_W3:01

SD_W [3:0]	Source power saving width[us	SD_W [3:01	Source power savng width [us]
0	Reserved	8	4
1	0.5	9	4.5
2	1	10	5
3	1.5	11	5.5
4	2	12	6
5	2.5[Default]	13	6.5
6	3	14	7
7	3.5	15	7.5

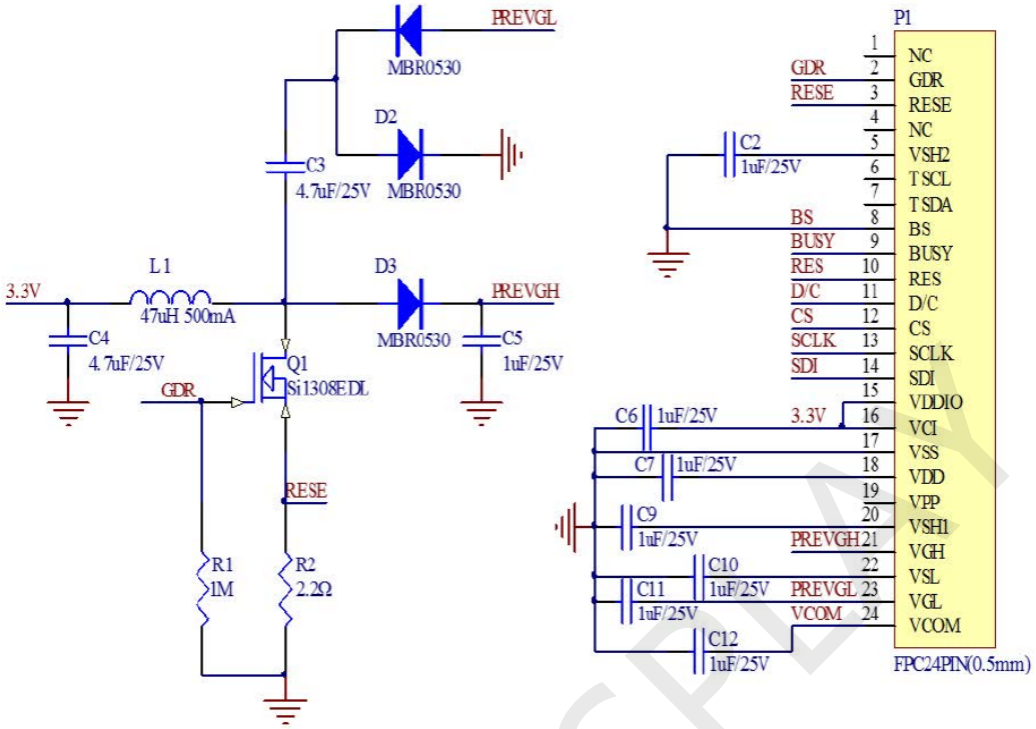
Remark:
VCOM_Wsetting<CDI setting
SD_Wseting<S2G setting

<table>
<tr><th>RN#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>E4</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>LVSEL</td><td>LVD Voltage Select Register
This command is sets for lowpower detect level power
A[1:0]=3h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A1</td><td>Ao</td><td></td><td>A[1:0]~LVD_SEL[1:0]
Lowpower detection threshold
00:2.2V
01:2.3V
10:2.4V
11:2.5V(Default)</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E6</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>TSSET</td><td>Manual input temperature value
This command is to force the TS value
A7:0]=00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>Az</td><td>As</td><td>As</td><td>A4</td><td>A3</td><td>Az</td><td>Ai</td><td>Ao</td><td></td><td>A7:0]-TS_SET[7:0]
When TSFIX=1,Temperature value wil beset by TS_SET[7:0].
Format of the temperature value is 8-bit binary value and it is 1degC per step.
<table>
<tr><th>TS_SET[7:0]</th><th>Foroe the TS Value(degC)</th></tr>
<tr><td>E7h</td><td>-25</td></tr>
<tr><td></td><td></td></tr>
<tr><td>FFh</td><td>-1</td></tr>
<tr><td>00h</td><td>0</td></tr>
<tr><td>01h</td><td>1</td></tr>
<tr><td></td><td></td></tr>
<tr><td>19h</td><td>25</td></tr>
<tr><td></td><td></td></tr>
<tr><td>31h</td><td>49</td></tr>
<tr><td>32h</td><td>50</td></tr>
</table></td></tr>
</table>

8.Block Diagram



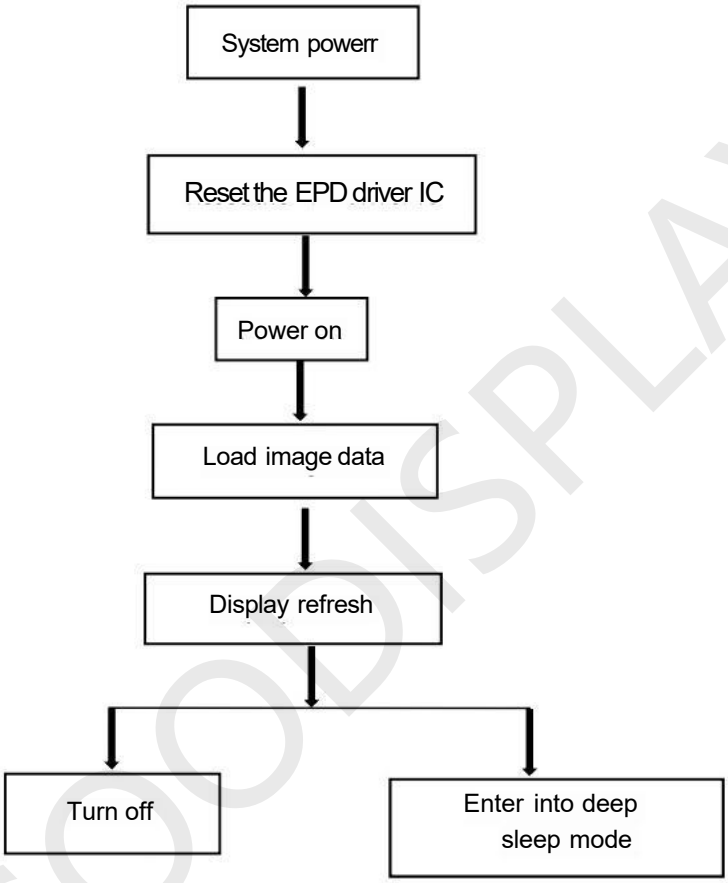
9.Typical Application Circuit with SPI Interface



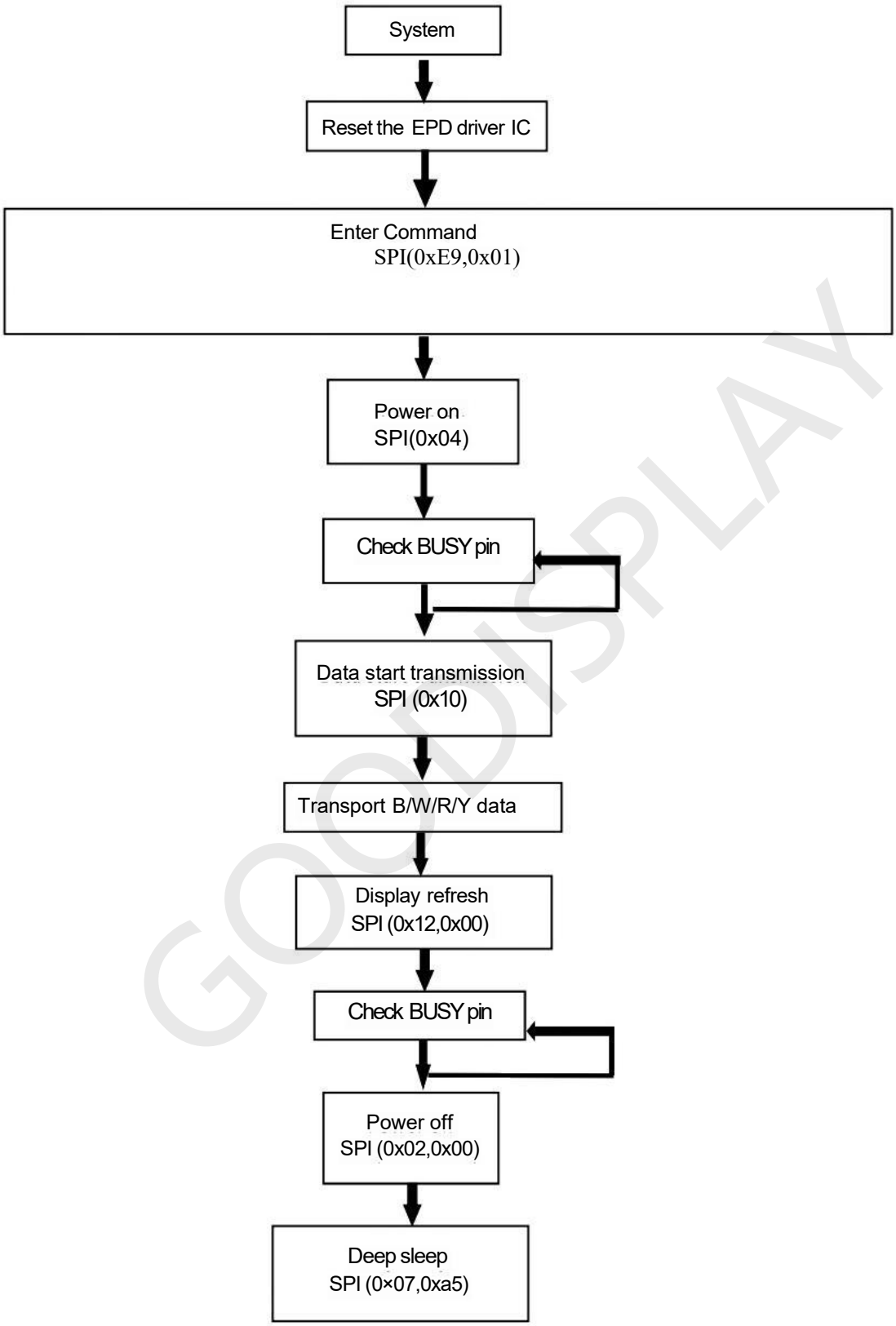
Part Name	Requirements for spare part
C1—C12	0603/0805; X5R/X7R;Voltage Rating:≥25V
R1、R2	0603/0805;1% variation,≥0.05W
D1—D3	MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV
Q1	Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ
L1	refer to NR3015: Io=500mA(max)
P1	24pins,0.5mm pitch

10.Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 OTP Operation Reference Program Code



11.Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C，500 h Test in white pattern
2	High-Temperature Storage	T=60°C，RH=35%，500h Test in white pattern
3	High-Temperature Operation	T=40°C，RH=35%， 500h
4	Low-Temperature Operation	0°C，500h
5	High-Temperature, High-Humidity Operation	T=40°C，RH=80%，500h
6	High-Temperature, High-Humidity Storage	T=60°C，RH=80%，500h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 100 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBMC:100pF;R:1.5k ohm) Contact+/-200V(MMC:200pF;R:0 ohm) (Naked EPD display,including IC and FPC area)
9	Vibration test	Frequency: 10-500Hz Direction: X, Y, Z Duration: 1 hour in each direction
10	Dropping test	The test height is determined by the weight of the test object. Weight ≤20KG, drop height 1000mm Weight ≤50KG, drop height 500mm Weight ≤100KG, drop height 250mm

Note:1.Stay white pattern for storage and non-operation test.

2.Operation is black→white→red→yellow pattern,the interval is 150s.

3.Put in 20℃-25℃ for 1hour after test finished,The function,appearance and display performance is OK.

12.Quality Assurance

12.1 Environment

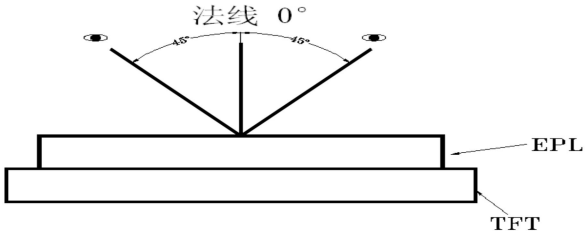
Temperature： 18~28℃

Humidity： 40%~70%RH

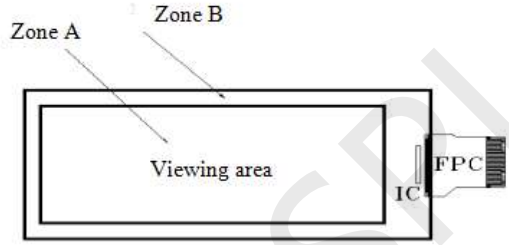
12.2 Illuminance

Brightness:800～1500LUX;Angle:Relate 45±5°surround;Function check when 150 ~ 200 LUX visual distance module surface 30CM

12.3 Inspect method



12.4 Display area



12.5 Ghosting test method

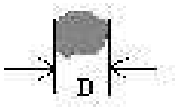
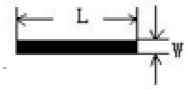
Four-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by maker.

1）Measurement Instruments：X-rite i1Pro

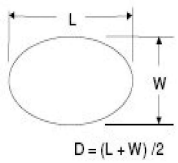
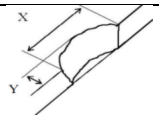
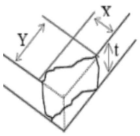
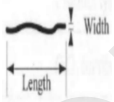
2）Ghosting formula: Refer to △E2000 calculation formula

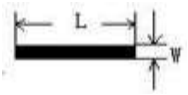
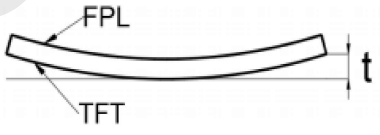
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection Visual/ Inspection card	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。 N≤4 allowable D＞0.4mm is not allowed	MI		
3	Black/White lines (No switch)	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed			
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm negligible 0.25mm＜D≤0.4mm N≤4 allowable D＞0.4mm is not allowed	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm And without affecting the electrode is permissible  2mm≤X or 2mm≤Y t= not counted.and without affecting the electrode , permissible  W≤0.1mm,L≤5mm, without affecting the electrode , n≤2	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.2mm, allow 0.2mm＜D≤0.35mm ,n≤4 allow D＞0.35mm is not allowed (n≤5 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤5.0mm。n≤5	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	
14	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC≤0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 t≤1.0mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) Good Display ‘s E-paper Display. And it is also added the functions of USB serial port, FLASH c hip, font chip, current detection ect.

Development Kit consists of the development board and the pinboard. Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32	https://www.good-display.com/product/219.html
ESP32	https://www.good-display.com/product/338.html
ESP8266	https://www.good-display.com/product/220.html
Arduino UNO	https://www.good-display.com/product/222.html

14.Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

15.Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5)If the EPD Panel/ Module is not refreshedevery 24 hours, aphenomena known as “Ghosting” or “ImageSticking” may occur.It is recommendedto refreshedtheESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue.

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance . Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:

https://www.good-display.com/news/80.html