



7.3 inch E-paper Display Series



GDEY073D46

Dalian Good Display Co., Ltd.

Product Specifications

Customer	Standard
Description	7.3" E-PAPER DISPLAY
Model Name	GDEY073D46
Date	2022/07/26
Revision	1.0

	Design Engineering		
	Approval	Check	Design
			

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CONTENTS

1. Overview.....	4
2. Features	4
3. Mechanical Specification.....	4
4. Mechanical Drawing of EPD Module.....	5
5. Input/output Interface.....	6
5.1 Pin Assignment.....	6
5.2 Panel Scan Direction.....	7
6. Typical Application Circuit.....	8

GOOD DISPLAY

1. Overview

GDEY073D46 is a reflective electrophoretic technology display module on an active matrix TFT substrate. The diagonal length of the active area is 7.3" and contains 800 x 480 pixels. The panel is capable of displaying 7-colors of black, white, red, yellow, blue, green, and orange images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

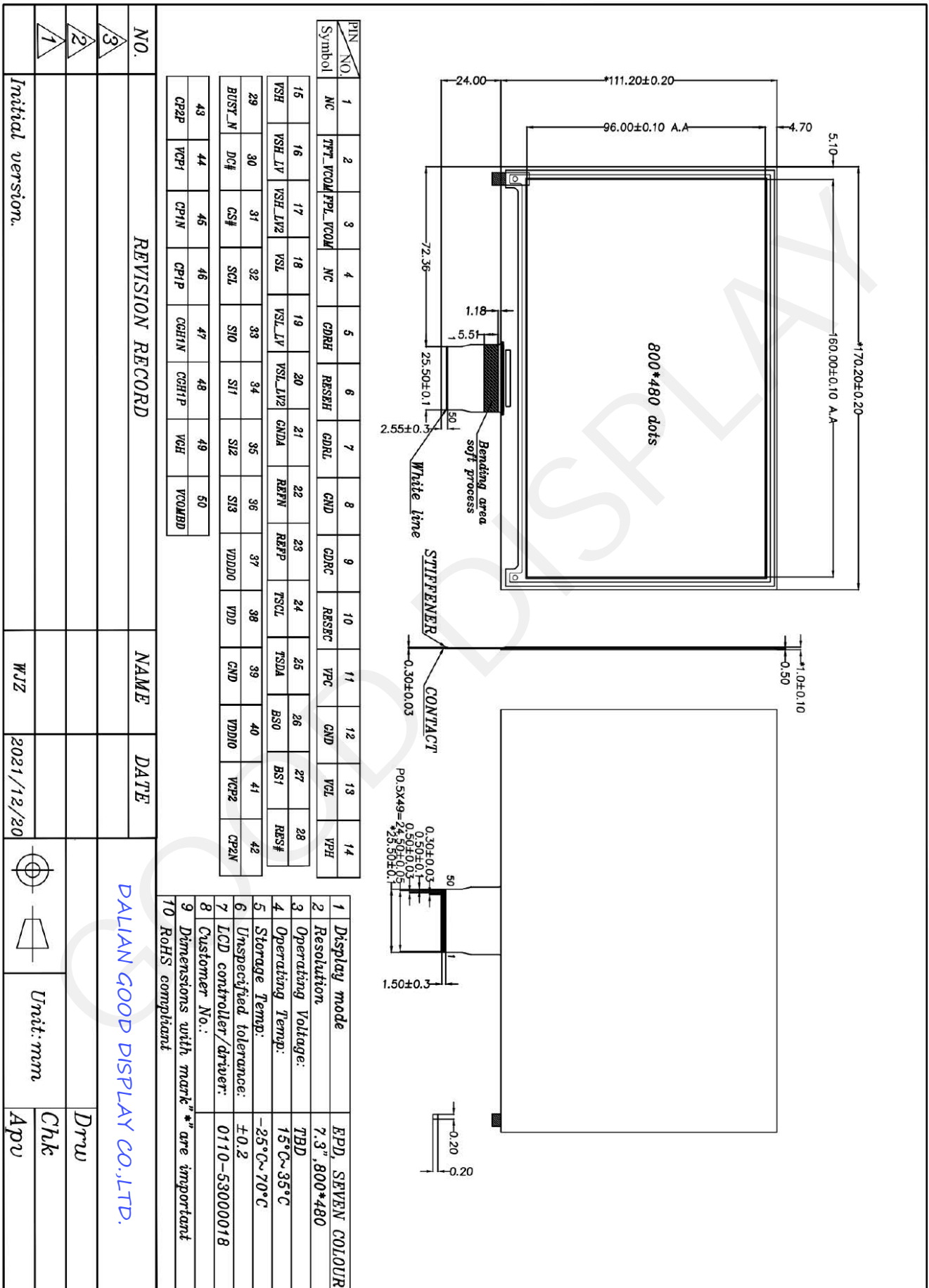
2. Features

- High contrast TFT electrophoretic
- 800 x 480 display
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Low current sleep mode
- On chip display RAM
- Serial peripheral interface available
- External SPI flash/EEPROM for waveform
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor
- Operational temperature range (15 ~ 35°C)

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.3	Inch	
Display Resolution	800(H)×480(V)	Pixel	Dpi:127
Active Area	160×96	mm	
Pixel Pitch	0.2×0.2	mm	
Pixel Configuration	Rectangle		
Outline Dimension	170.2(H)×111.2 (V) ×1.0(D)	mm	
Weight	TBD	g	

4. Mechanical Drawing of EPD module



5. Input /Output Interface

5.1 Pin Assignment

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	
2	P	TFT_VCOM	TFT_VCOM driving voltage	
3	P	FPL_VCOM	FPL_VCOM driving voltage	
4		NC	NC	
5	I/O	GDRH	N-Channel MOSFET Gate Drive Control	
6	I/O	RESEH	Current Sense Input for the Control Loop	
7		GDRL	Reserved	
8	P	GND	Ground	
9	I/O	GDRC	P-Channel MOSFET Gate Drive Control	
10	I/O	RESEC	Current Sense Input for the Control Loop	
11	P	VPC	VPC driving voltage	
12	P	GND	Ground	
13	P	VGL	Negative Gate driving voltage	
14	P	VPH	VPH driving voltage	
15	P	VSH	Positive Source driving voltage	
16	P	VSH_LV	Positive Source driving voltage	
17	P	VSH_LV2	Positive Source driving voltage	
18	P	VSL	Negative Source driving voltage	
19	P	VSL_LV	Negative Source driving voltage	
20	P	VSL_LV2	Negative Source driving voltage	
21	P	GND	Ground ; Connect to GND	
22		REFN	Reserved	
23		REFP	Reserved	
24	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
25	I/O	TSDA	I2C Interface to digital temperature sensor Data pin	
26	I	BS0	Bus selection pin; L: 4-wire IF. H: 3-wire IF. (Default)	
27	I	BS1	Bus selection pin; L: refer to BS0. (Default) H: Standard 4-wire SPI/dual SPI/quad SPI	
28	I	RES#	Reset	
29	O	BUSY_N	Busy state output pin	
30	I	D/C#	Data /Command control pin (D/C)	
31	I	CS#	Chip Select input pin (CSB)	
32	I	SCL	Serial clock pin (SPI)	
33	I/O	SI0	serial data pin (SPI)	
34	I/O	SI1	serial data pin ; Reserved	
35	I/O	SI2	serial data pin ; Reserved	
36	I/O	SI3	serial data pin ; Reserved	
37	P	VDDDO	Core logic power pin; Connect to VDDD	

38	P	VDD	Supply voltage	
39	P	GND	Ground; Connect to GNDA	
40	P	VDDIO	Supply voltage	
41	P	VCP2	Charge Pump Pin	
42	P	CP2N	Charge Pump Pin	
43	P	CP2P	Charge Pump Pin	
44	P	VCP1	Charge Pump Pin	
45	P	CP1N	Charge Pump Pin	
46	P	CP1P	Charge Pump Pin	
47		CGH1N	Charge Pump Pin; Reserved	
48		CGH1P	Charge Pump Pin; Reserved	
49	P	VGH	Positive Gate driving voltage	
50	P	VCOMBD	VCOMBD driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY_N) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

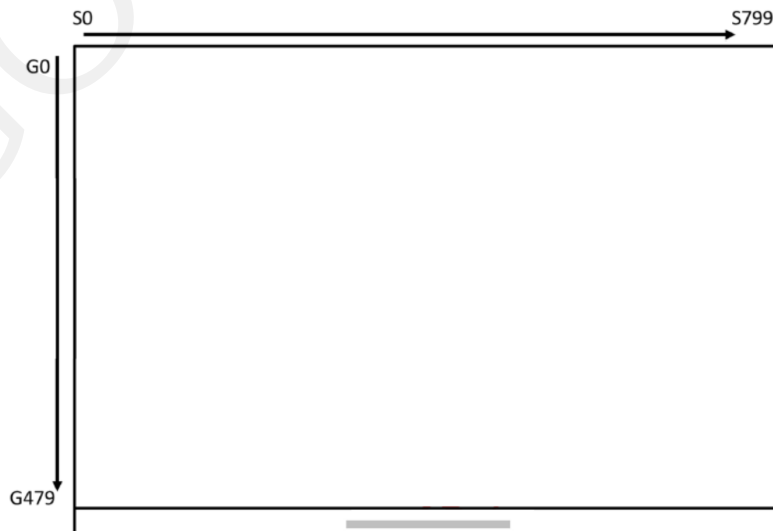
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS0) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

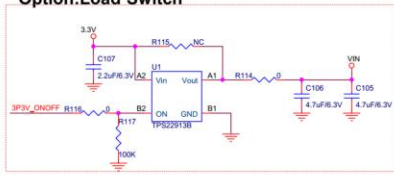
BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

5.2 Panel Scan Direction

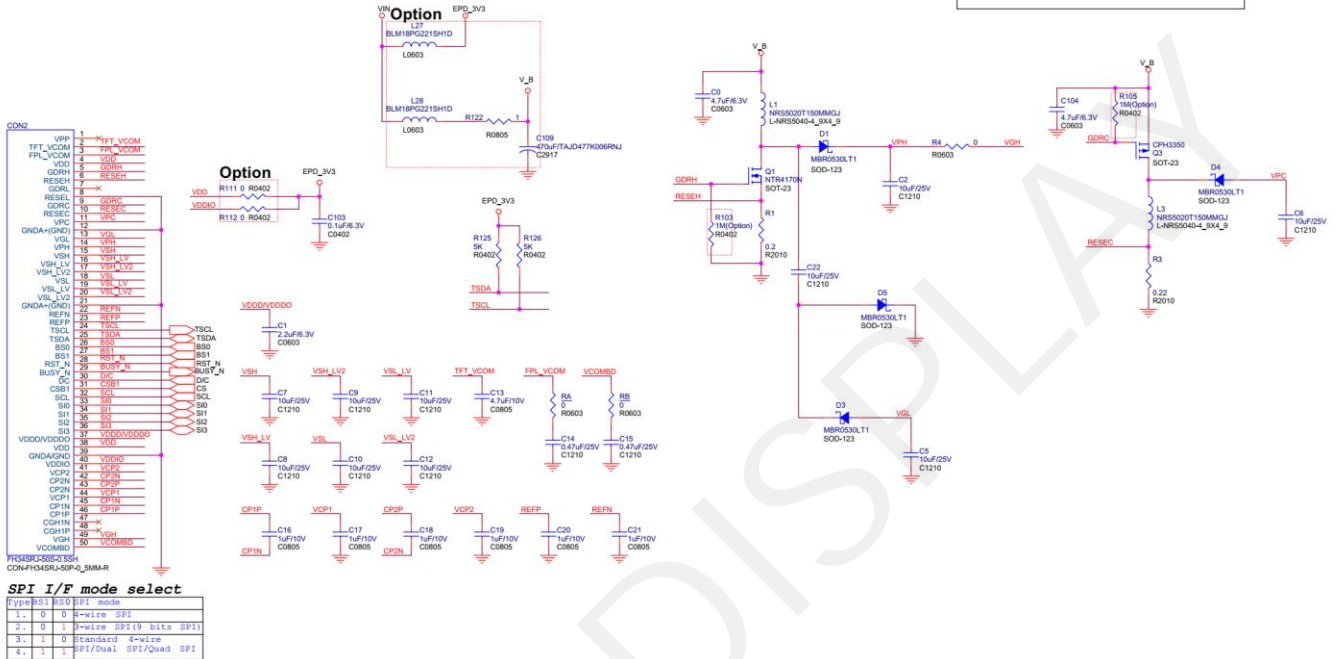
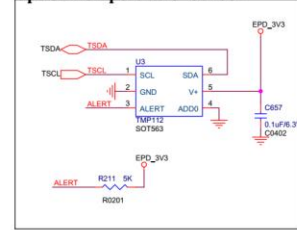


6. Typical Application Circuit

Option:Load Switch



Option:Temperature Sensor



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SPI I/F mode select
Fyp#R31 R30 SPI mode
1. 0 0 4-wire SPI
2. 0 1 3-wire SPI(9 bits SPI)
3. 1 0 Standard 4-wire
4. 1 1 SPI/Dual SPI/Quad SPI
    
```

Item	Quantity	Reference	Part	PCB Footprint
1	1	CON2	FH34SRJ-50S-0.5SH	CON-FH34SRJ-50P-0_5MM-R
2	4	C104,C105,C106,C0	4.7uF/6.3V	C0603
3	2	C1,C107	2.2uF/6.3V	C0603
4	10	C2,C5,C6,C7,C8,C9,C10,C11,C12,C22	10uF/25V	C1210
5	1	C13	4.7uF/10V	C0805
6	2	C14,C15	0.47uF/25V	C1210
7	6	C16,C17,C18,C19,C20,C21	1uF/10V	C0805
8	2	C103,C657	0.1uF/6.3V	C0402
9	1	C109	470uF/TAJD477K006RNJ	C2917
10	4	D1,D3,D4,D5	MBR0530LT1	SOD-123
11	2	L1,L3	NRS5020T150MMGJ	L-NRS5040-4_9X4_9
12	2	L27,L28	BLM18PG221SH1D	L0603
13	1	Q1	NTR4170N	SOT-23
14	1	Q3	CPH3350	SOT-23
15	3	R4,RB,RA		0 R0603
16	1	R1		0.2 R2010
17	1	R3		0.22 R2010
18	2	R103,R105	1M(Option)	R0402
19	3	R111,R112,R116		0 R0402
20	1	R114		0 R1206
21	1	R115	NC	R0603
22	1	R117		R0402
23	1	R122		1 R0805
24	2	R125,R126	5K	R0402
25	1	R211	5K	R0201
26	1	U1	TPS22913B	BGA-4P-0_5MM-0_9X0_9
27	1	U3	TMP112	SOT563