7.5 inch
E-paper Display Series

GooDisplay®

GDEY075T7

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**7.5” E-PAPER DISPLAY**
Model Name	**GDEY075T7**
Date	**2021/03/10**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
			

Zhongnan Building, No.18, Zhonghua West ST,Ganjingzi DST,Dalian,CHINA
Tel: +86-411-84619565
Email: info@good-display.com
Website: www.good-display.com

REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	MAR.10.2021	New Creation	ALL	

CONTENTS

1.Over View

GDEY075T7 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The7.5” active area contains 800×480 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

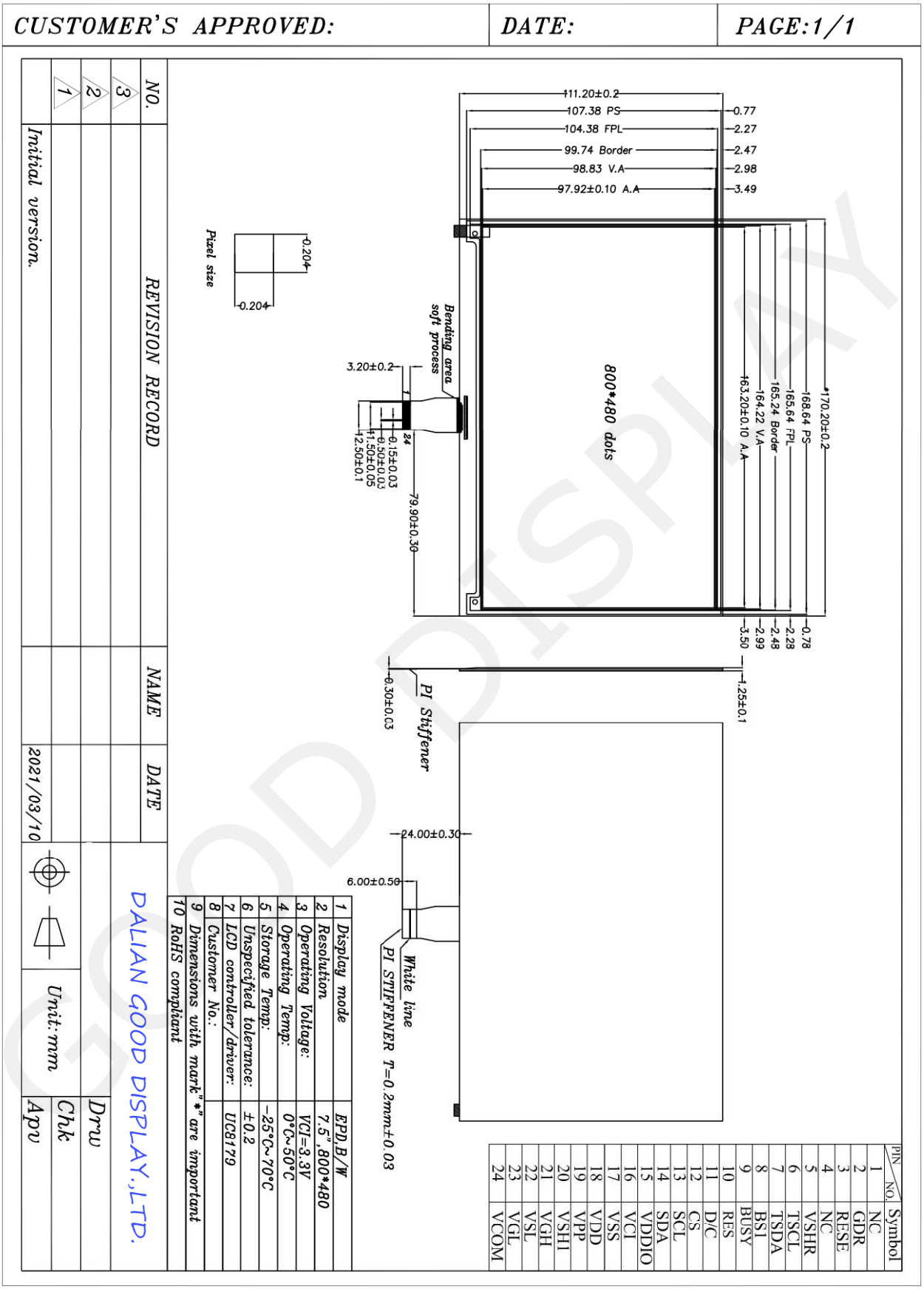
2.Features

- 800×480 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in flash memory
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM,Gate and
- Source driving voltage
- I2C Signal Master Interface to read external temperature sensor/ built-in temperature sensor
- Available in COG package IC thickness 300um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	800 (H)×480(V)	Pixel	Dpi:124
Active Area	163.20(H)×97.92(V)	mm	
Pixel Pitch	0.204×0.204	mm	
Pixel Configuration	Square		
Outline Dimension	170.20(H)×111.20 (V) ×1.25 (D)	mm	
Weight	44±0.5	g	

4. Mechanical Drawing of EPD module



5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSHR	C	Positive Source driving voltage(Red)	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES	I	Reset signal input. Active Low.	Note 5-3
11	D/C	I	Data /Command control pin	Note 5-2
12	CS	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 5-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RST) is reset signal input. The Reset is active Low
Note 5-4: This pin (BUSY) is BUSY state output pin. When BUSY is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put BUSY pin low when the driver IC is working such as:

Outputting display waveform; or

Programming with OTP

Communicating with digital temperature sensor

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

Table: Bus interface selection

6.Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VCI +0.3	V
Operating Temp range	TOPR	0 to +50	°C
Storage Temp range	TSTG	-25 to+70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables

6.2 DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.5	3.3	3.6	V
Core logic voltage	V_{DD}		VDD	2.5	3.3	3.6	V
High level input voltage	V_{IH}	-	-	0.7 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.3 V_{CI}	V
High level output voltage	V_{OH}	IOH = -400uA	-	VCI-0.4	-	-	V
Low level output voltage	V_{OL}	IOL = 400uA	-	0	-	0.4	V
Typical operating current	Iopr_V_{CI}	V_{CI} =3.3V	-	-	8	12	mA
Image update time	-	25 ºC	-	-	3	-	sec
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	25		uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	2	5	uA

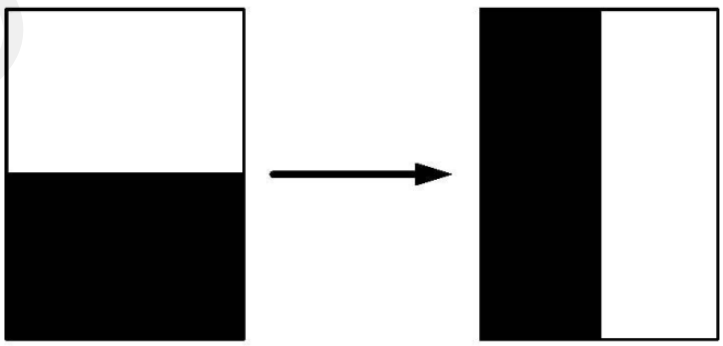
Notes:

1. The typical power is measured with following transition from horizontal 2 scale pattern to

vertical 2 scale pattern.

2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by GOOD DISPLAY



6.3 AC Characteristics

6.3.1 MCU Interface Selection

Provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

6.3.2 3 wire SPI format.

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

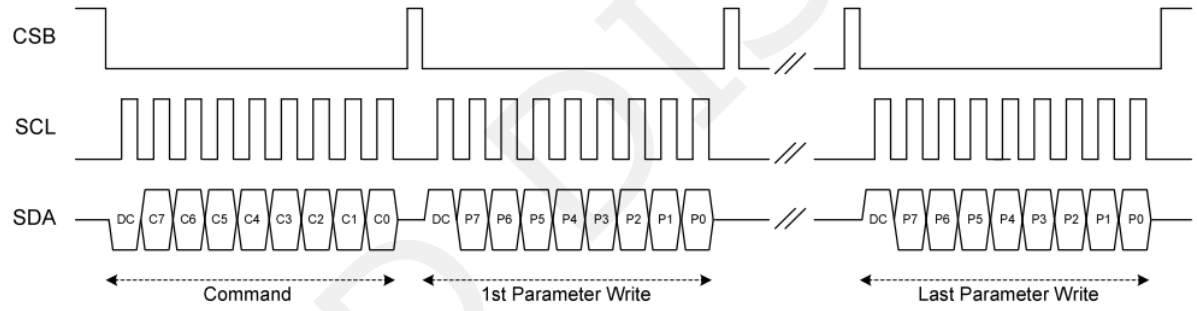


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

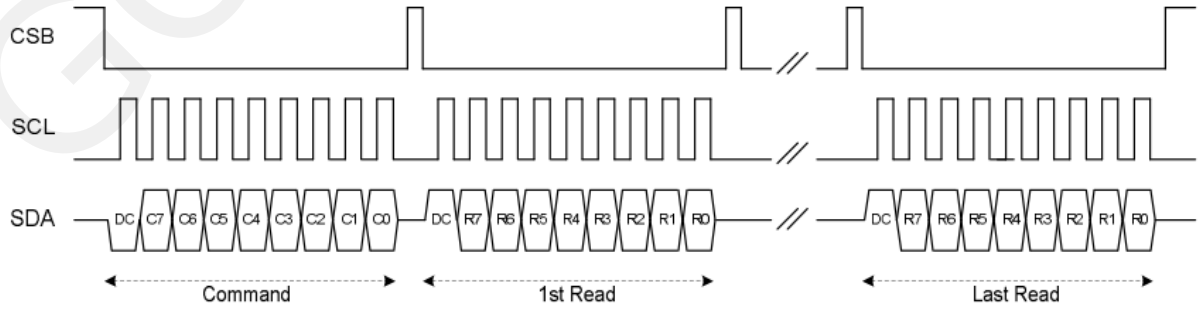


Figure: 3-wire SPI read operation

6.3.3 4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

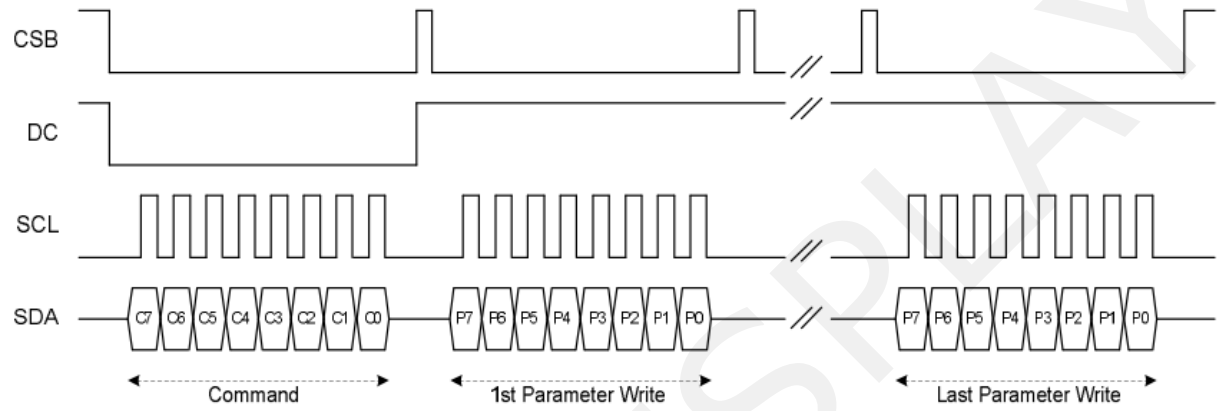


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

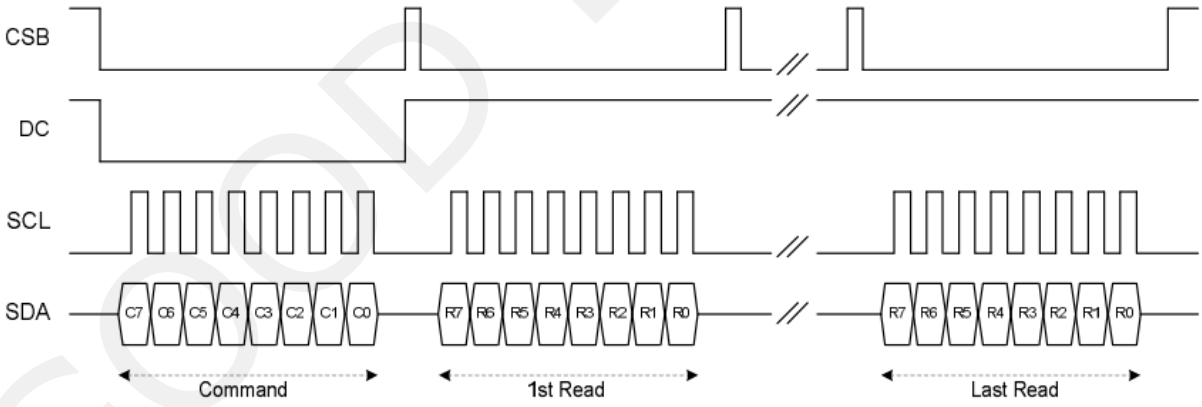


Figure: 4-wire SPI read operation

6.3.4 3 wire dual SPI format.

Data / Command is recognized with the first bit transferred at SDA. Data are transferred in the unit of 5 SPI clocks. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 5 SPI clocks. (The serial counter is reset at the rising edge of the CSB signal.) In 3-wire dual SPI mode, SDA and SDA1 are only input mode for data write transmission.

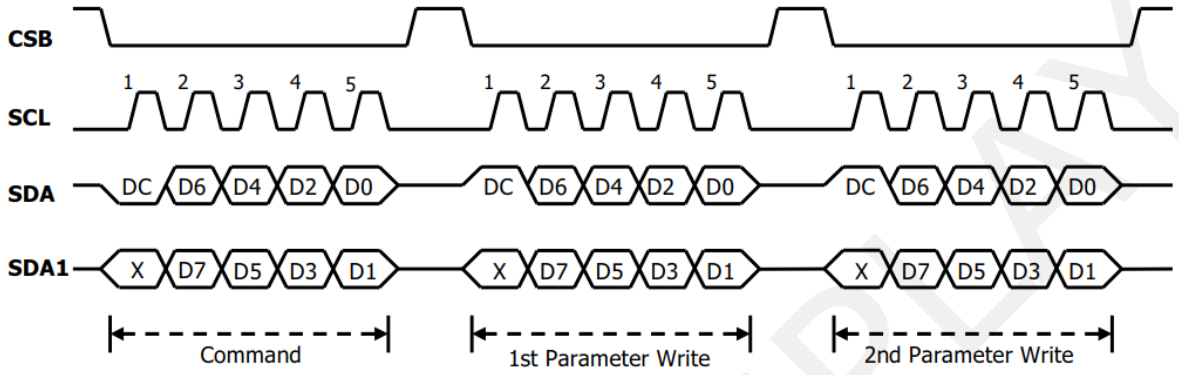


Figure: 3-wire dual SPI write operation

6.3.5 4 wire dual SPI format.

Data / Command is recognized with DC pin. Data are transferred in the unit of 4 SPI clocks. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 4 SPI clocks. (The serial counter is reset at the rising edge of the CSB signal.) In 4-wire dual SPI mode, SDA and SDA1 are only input mode for data write transmission.

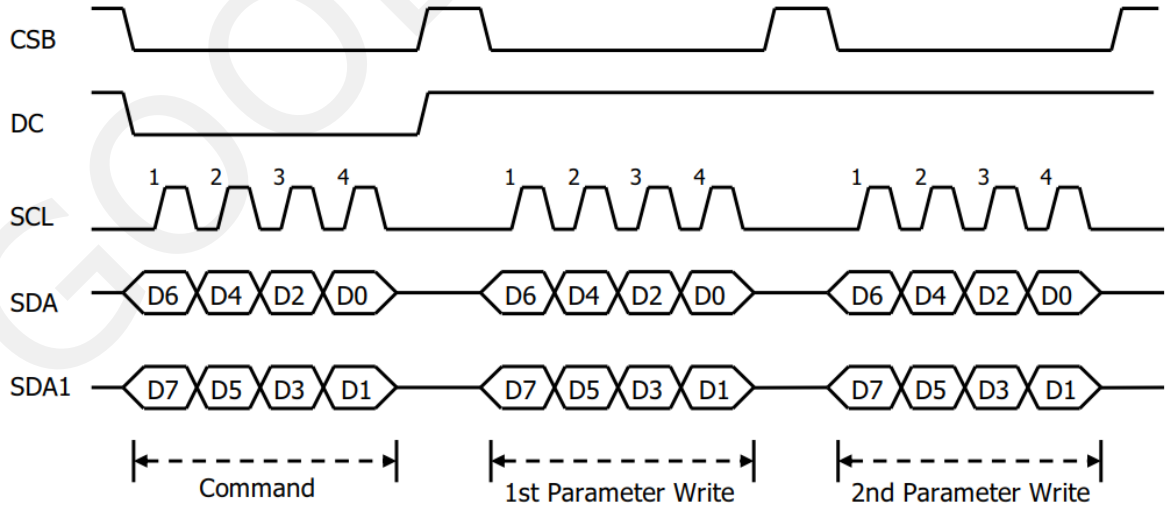


Figure: 4-wire dual SPI write operation

6.4 Timing Characteristics.

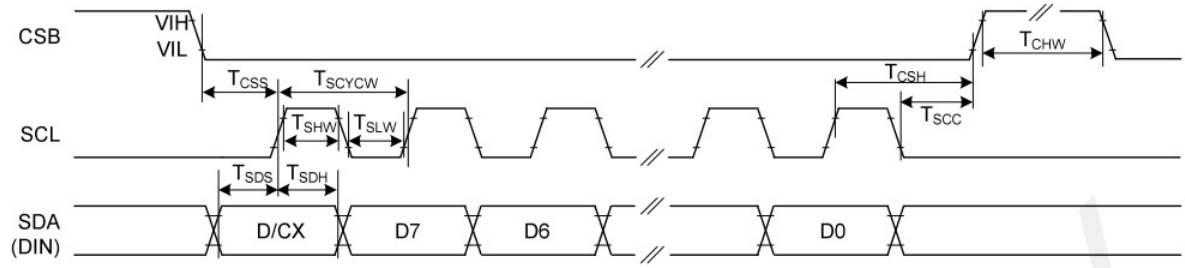


Figure: 3-wire Serial Interface Characteristics (Write mode)

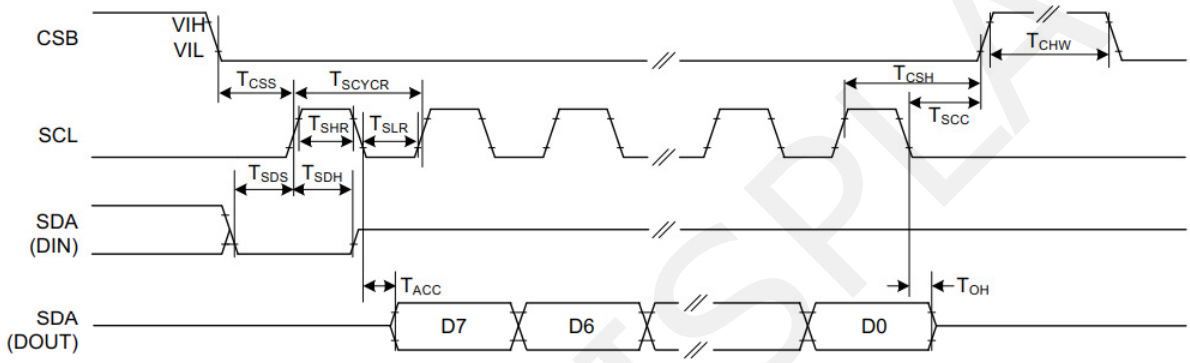


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	230			ns
T_{SHR}		SCL "H" pulse width (Read)	60			ns
T_{SLR}		SCL "L" pulse width (Read)	60			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			230	ns
T_{OH}		Output disable time	15			ns

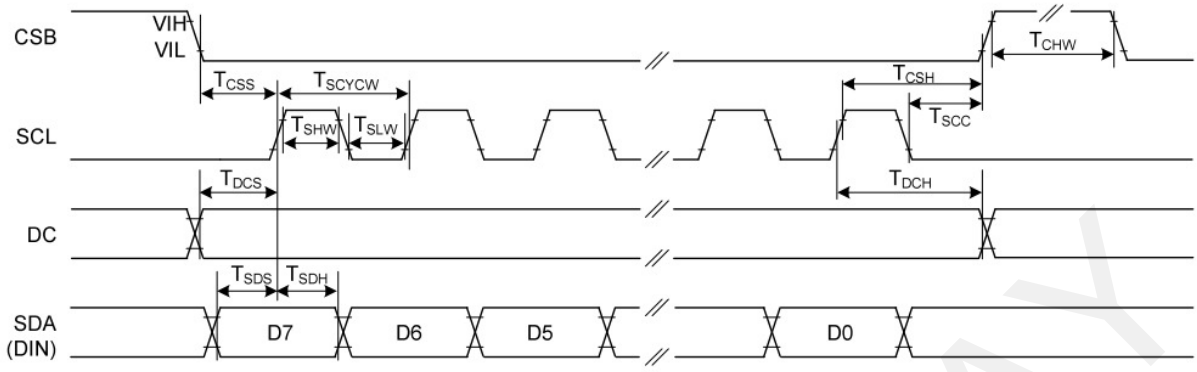


Figure: 4-wire Serial Interface Characteristics (Write mode)

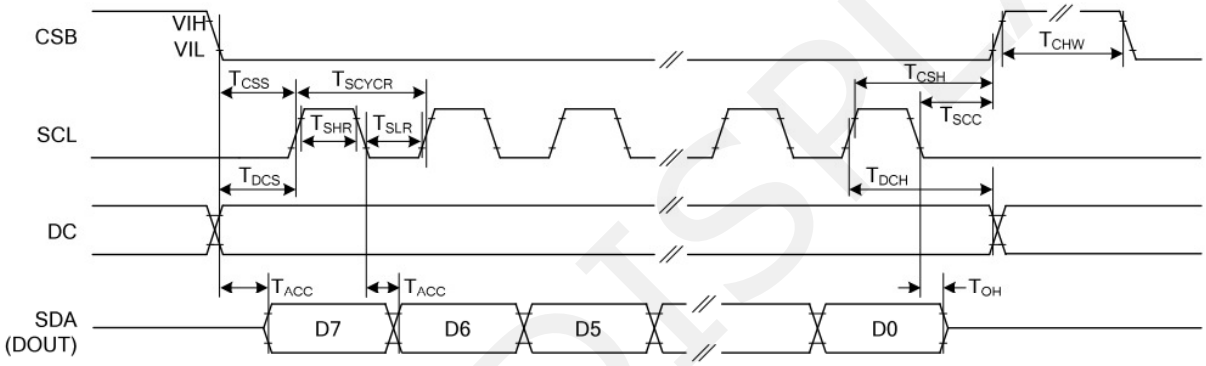


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	230			ns
T_{SHR}		SCL "H" pulse width (Read)	60			ns
T_{SLR}		SCL "L" pulse width (Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			230	ns
T_{OH}		Output disable time	15			ns

7. Command Table

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	--	--	#	#	#	#	#	#	REG, KW/R, UD, SHL, SHD_N, RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	#	--	#	#	#	BD_EN, VSR_EN, VS_EN, VG_EN	07H
		0	1	--	--	--	#	--	#	#	#	VCOM_SLEW, VG_LVL[2:0]	17H
		0	1	--	--	#	#	#	#	#	#	VDH_LVL[5:0]	3AH
		0	1	--	--	#	#	#	#	#	#	VDL_LVL[5:0]	3AH
		0	1	--	--	#	#	#	#	#	#	VDHR_LVL[5:0]	03H
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC1[5:0]	17H
		0	1	#	--	#	#	#	#	#	#	PHC2_EN, BT_PHC2[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data (800x600):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-7:n]	-
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (800x600):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-7:n]	-
13	Dual SPI	0	0	0	0	0	1	0	1	0	1		15H
		1	1	--	--	#	#	--	--	--	--	MM_EN, DUSPI_EN	00H
14	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
15	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
16	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
17	K2W LUT (LUTKW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
18	W2K LUT (LUTWK / LUTW) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
19	K2K LUT (LUTKK / LUTK) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
20	Border LUT (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1		25H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
21	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	#	--	--	--	--	--	--	STATE_XON[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
22	KW LUT option (KWOPT)	0	0	0	0	1	0	1	0	1	1		2BH
		0	1	--	--	--	--	--	--	#	#	ATRED, NORED	00H
		0	1	#	#	--	--	--	--	--	--	KWE[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	KWE[7:0]	00H
23	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	--	--	#	#	#	#	FRS[3:0]	06H
24	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
25	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
26	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
27	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43H
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
28	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44H
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
29	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50H
		0	1	#	--	#	#	--	--	#	#	BDZ, BDV[1:0], DDX[1:0]	31H
		0	1	--	--	--	--	#	#	#	#	CDI[3:0]	07H

31	End Voltage Setting (EVS)	0	0	0	1	0	1	0	0	1	0		52H
		0	1	--	--	--	--	#	--	#	#	VCEND, BDEND[1:0]	02H
32	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
33	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	--	--	--	--	--	--	#	#	HRES[9:8]	03H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	20H
		0	1	--	--	--	--	--	--	#	#	VRES[9:0]	02H
		0	1	#	#	#	#	#	#	#	#		58H
34	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	--	--	--	--	--	--	#	#	HST[9:8]	00H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	#	#	VST[9:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
35	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		1	1	#	#	#	#	#	#	#	#	PROD_REV[23:16]	FFH
		1	1	#	#	#	#	#	#	#	#	PROD_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	PROD_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:16]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	0CH
36	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
37	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
38	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
39	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H
40	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	--	--	--	--	--	--	#	#	HRST[9:8]	00H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	--	--	--	--	--	--	#	#	HRED[9:8]	03H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	1FH
		0	1	--	--	--	--	--	--	#	#	VRST[9:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	#	#	VRED[8:0]	02H
		0	1	#	#	#	#	#	#	#	#		57H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
41	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
42	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
43	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
44	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
45	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
46	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
47	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
48	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
49	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H
50	Temperature Boundary Phase-C2 (TSBDRY)	0	0	1	1	1	0	0	1	1	1		E7H
		0	1	#	#	#	#	#	#	#	#	TSBDRY_PHC2[7:0]	00H

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00H
	0	1	-	-	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	BD_EN	-	VSR_EN	VS_EN	VG_EN	07H
	0	1	-	-	-	VCOM _SLEW	-	VG_LVL[2:0]			17H
	0	1	-	-	VDH_LVL[5:0]						3AH
	0	1	-	-	VDL_LVL[5:0]						3AH
	0	1	-	-	VDHR_LVL[5:0]						03H

BD_EN: Border LDO enable
0 : Border LDO disable (Default)
Border level selection: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR
1 : Border LDO enable
Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b:VBL(VCOM-VDH) 11b: VDHR

VSR_EN: Source LV power selection
0 : External source power from VDHR pins
1 : Internal DC/DC function for generating VDHR. (Default)

VS_EN: Source power selection
0 : External source power from VDH/VDL pins
1 : Internal DC/DC function for generating VDH/VDL. (Default)

VG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_SLEW: VCOM slew rate selection for voltage transition. The value is fixed at "**1**".

VG_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 **(Default)**	VGH=20V, VGL= -20V

VDH_LVL[5:0]: Internal VDH power selection for K/W pixel.(**Default value: 111010b**)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	**111010**	**14.0 V**
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

VDL_LVL[5:0]: Internal VDL power selection for K/W pixel. (**Default value: 111010b**)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	100110	-10.0 V	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	**111010**	**-14.0 V**
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

VDHR_LVL[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 000011b**)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	**3.0 V**	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Internal Bandgap Set	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Booster Software Start Set	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA[7:6]		BT_PHA[5:3]			BT_PHA[2:0]			17H
	0	1	BT_PHB[7:6]		BT_PHB[5:3]			BT_PHB[2:0]			17H
	0	1	-	-	BT_PHC1[5:3]			BT_PHC1[2:0]			17H
	0	1	PHC2EN	-	BT_PHC2[5:3]			BT_PHC2[2:0]			17H

BT_PHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHC1[5:3]: Driving strength of phase C1

000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BT_PHC1[2:0]: Minimum OFF time setting of GDR in phase C1

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

PHC2EN: **Booster phase-C2 enable**

0: Booster phase-C2 disable
Phase-C1 setting always is applied for booster phase-C.

1: Booster phase-C2 enable
If temperature > temperature boundary phase-C2(RE7h[7:0]), phase-C1 setting is applied for booster phase-C.
If temperature <= temperature boundary phase-C2(RE7h[7:0]), phase-C2 setting is applied for booster phase-C.

BT_PHC2[5:3]: Driving strength of phase C2

000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BT_PHC2[2:0]: Minimum OFF time setting of GDR in phase C2

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “K/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.

(13) DUAL SPI MODE (DUSPI) (R15H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	1	0	1	15H
	0	1	-	-	MM_EN	DUSPI_EN	-	-	-	-	00H

This command sets dual SPI mode.

MM_EN: MM input pin definition enable.

0: MM input pin definition disable
1: MM input pin definition enable.

DUSPI_EN: Dual SPI mode enable.

0: Dual SPI mode disable (single SPI mode)
1: Dual SPI mode enable

(14) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(15) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores VCOM Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:

D[7:6], D[5:4], D[3:2], D[1:0]: Level Selection

00b: VCOM_DC
01b: VDH+VCOM_DC (VCOMH)
10b: VDL+VCOM_DC (VCOML)
11b: Floating

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:

Number of Frames

0000 0000b: 0 frame
: :
1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:

Times to Repeat

0000 0000b: 0 time
: :
1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.
If KW/R=1 (KW mode), only 7 groups are used.

(16) W2W LUT (LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38:

Level Selection.

00b: GND
01b: VDH
10b: VDL
11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:

Number of Frames

0000 0000b: 0 frame
: :
1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43:

Times to Repeat

0000 0000b: 0 time
: :
1111 1111b: 255 times

If KW/R=0 (KWR mode), LUTWW is not used.
If KW/R=1 (KW mode), LUTWW is used.

(17) K2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for K2W or Red (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0	22H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:

Level Selection.

00b: GND
01b: VDH
10b: VDL
11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:

Number of Frames

0000 0000b: 0 frame
: :
: :
1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:

Times to Repeat

0000 0000b: 0 time
: :
: :
1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

(18) W2K LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

(19) K2K LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

(20) BORDER LUT (LUTBD) (R25H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for Border (43-byte command, Bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1	25H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38:

Level selection.

BD_EN=0:	00b: VCOM	01b: VDH	10b: VDL	11b: VDHR
BD_EN=1:	00b: VCOM	01b: VBH(VCOM-VDL)	10b: VBL(VCOM-VDH)	11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43:

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Only 7 LUTBD groups are used in KW mode or KWR mode.

(21) LUT OPTION (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	0	0	1	0	1	0	1	0	2AH
	0	1	STATE_XON[9:8]		-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H

This command sets XON control enable.

STATE_XON[9:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

00 0000 0000b: no All-Gate-ON

00 0000 0001b: State-1 All-Gate-ON

00 0000 0011b: State-1 and State2 All-Gate-ON

(22) KW LUT Option (KWOPT) (R2BH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
KW LUT Option	0	0	0	0	1	0	1	0	1	1	2BH
	0	1	-	-	-	-	-	-	ATRED	NORED	00H
	0	1	KWE[9:8]		-	-	-	-	-	-	00H
	0	1	KWE[7:0]								00H

This command sets KW LUT mechanism option in KWR mode's LUT and only valid in K/W/R mode.

{ATRED, NORED}: KW LUT or KWR LUT selection control

ATRED	NORED	Description
0	0	KWR LUT always
0	1	KW LUT only
1	0	Auto detect by red data
1	1	KW LUT only

KWE[9:0]:

KW LUT enable control bits. Each bit controls one state, KWE[0] for state-1, KWE[1] for state-2, … .

At least 1 Enable Control bit should be set when KW LUT only is selected in KWR mode.

00 0000 0001b: KW LUT enable in State-1

00 0000 0011b: KW LUT enable in State-1 and State2

00 0000 1011b: KW LUT enable in State-1, State2 and State-4

(23) PLL Control (PLL) (R30H)

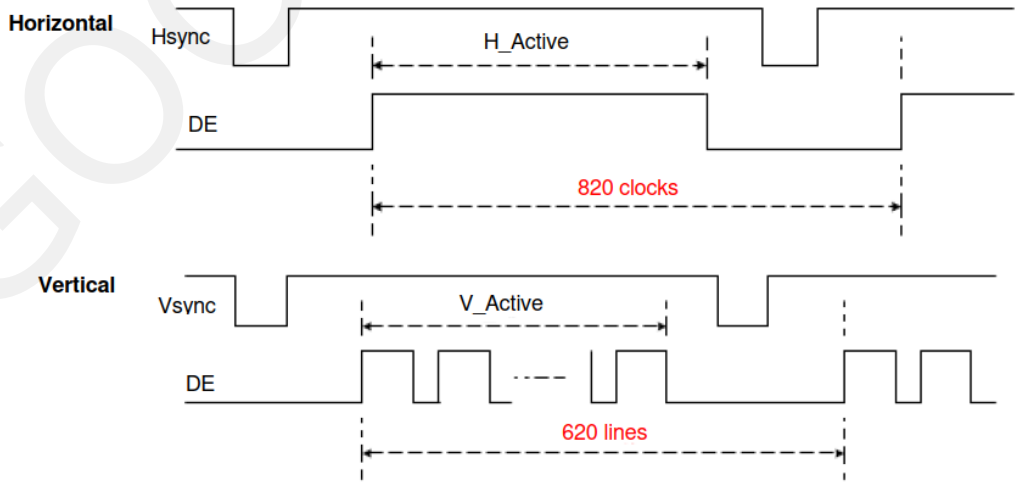
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	-	FRS[3:0]				06H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[3:0]: Frame rate setting

FRS	Frame rate
0000	5Hz
0001	10Hz
0010	15Hz
0011	20Hz
0100	30Hz
0101	40Hz
0110	**50Hz**
0111	60Hz

FRS	Frame rate
1000	70Hz
1001	80Hz
1010	90Hz
1011	100Hz
1100	110Hz
1101	130Hz
1110	150Hz
1111	200Hz



(24) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	0	1	0	0	0	0	0	0	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temp. (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temp. (°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(25) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	0	1	0	0	0	0	0	1	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calibration
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calibration
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(26) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I^2C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(27) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(28) PANEL GLASS CHECK (PBC)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	0	0	0	1	0	0	0	1	0	0	44H
	1	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(29) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	BDZ	-	BDV[1:0]		N2OCP	-	DDX[1:0]		31h
	0	1	-	-	-	SDEND	CDI[3:0]				07H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

BDZ: Border Hi-Z control

0: Border output Hi-Z disabled (default) 1: Border output Hi-Z enabled

BDV[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

N2OCP: Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default) 1: Copy NEW data to OLD data enabled

DDX[1:0]: Data polarity.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

SDEND: source driving ending

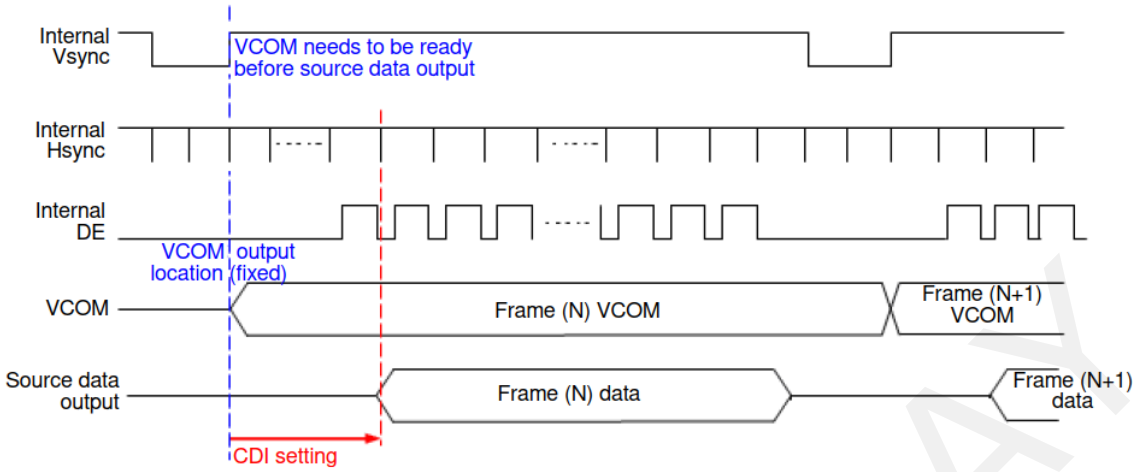
0: source driver channels output 2-frame 0V at the end

1: source driver channels keep the last state at the end

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



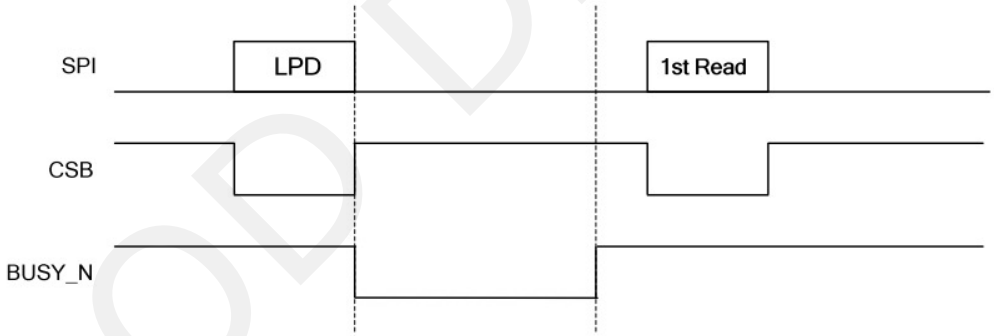
(30) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD} < 2.5V, 2.4V, 2.3V, or 2.2V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(31) END VOLTAGE SETTING (EVS) (R52H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
End Voltage Setting	0	0	0	1	0	1	0	0	1	0	52h
	0	1	-	-	-	-	VCEND	-	BDEND[1:0]		02h

This command selects source end voltage and border end voltage after LUTs are finished.

VCEND: VCOM end voltage selection

0b: VCOM_DC 1b: floating

BDEND[1:0]: Border end voltage selection

00b: 0V 01b: 0V **10b: VCOM_DC** 11b: floating

(32) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

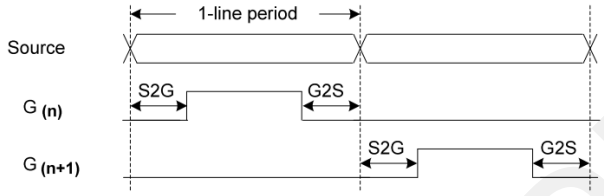
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 667 nS.



(33) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	-	-	-	-	-	-	HRES[9:8]		03h
	0	1	HRES[7:3]					0	0	0	20h
	0	1	-	-	-	-	-	-	VRES[9:8]		02h
	0	1	VRES[7:0]								58h

This command defines resolution setting.

HRES[9:3]: Horizontal Display Resolution (Value range: 01h ~ 64h)

VRES[9:0]: Vertical Display Resolution (Value range: 001h ~ 258h)

Active channel calculation, assuming HST[9:0]=0, VST[9:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[9:0] – 1

Source: First active source = S0;
Last active source = HRES[9:3]*8 – 1

Example: 128 (source) x 272 (gate), assuming HST[9:0]=0, VST[9:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[9:0] = 272, 272 – 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[9:3]=16, 16*8 – 1 = 127)

(34) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	-	-	-	-	-	-	HST[9:8]		00h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	VST[9:8]		00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[9:3]: Horizontal Display Start Position (Source). (Value range: 00h ~ 63h)

VST[9:0]: Vertical Display Start Position (Gate). (Value range: 000h ~ 257h)

Example : For 128(Source) x 240(Gate)
HST[9:3] = 4 (HST[9:0] = 4*8 = 32),
VST[9:0] = 32

Gate: First active gate = G32 (VST[9:0] = 32),
Last active gate = G271 (VRES[9:0] = 240, VST[9:0] = 32, 240-1+32=271)

Source: First active source = S32 (HST[9:0]= 32),
Last active source = S239 (HRES[9:0] = 128, HST[9:0] = 32, 128-1+32=239)

(35) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	PROD_REV[23:16]								FFh
	1	1	PROD_REV[15:8]								FFh
	1	1	PROD_REV[7:0]								FFh
	1	1	LUT_REV[23:16]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[7:0]								FFh
	1	1	CHIP_REV[7:0]								0Ch

The command reads the product revision, LUT revision and chip revision.

PROD_REV[23:0]: Product Revision. PROD_REV[23:0] is read from OTP address 0x0BDD ~ 0X0BDF or 0x17DD ~ 0x17DF.

LUT_REV[23:0]: LUT Revision. LUT_REV[23:0] is read from OTP address 0x0BE0 ~ 0X0BE2 or 0x17E0.~ 0x17E2.

CHIP_REV[7:0]: Chip Revision, fixed at 00001100b.

(36) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ Flag	I²C_ERR	I²C_ BUSYN	Data_ Flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_Flag: Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

Data_Flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(37) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command triggers auto VCOM sensing mechanism.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(38) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(39) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(40) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	1	0	0	0	0	90h
	0	1	-	-	-	-	-	-	HRST[9:8]		00h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	HRED[9:8]		03h
	0	1	HRED[7:3]					1	1	1	1Fh
	0	1	-	-	-	-	-	-	VRST[9:8]		00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	VRED[9:8]		02h
	0	1	VRED[7:0]								57h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[9:3]: Horizontal start channel bank. (Value range: 00h~63h)

HRED[9:3]: Horizontal end channel bank. (Value range: 00h~63h). HRED must be greater than HRST.

VRST[9:0]: Vertical start line. (Value range: 000h~257h)

VRED[9:0]: Vertical end line. (Value range: 000h~257h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(41) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(42) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(43) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(44) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

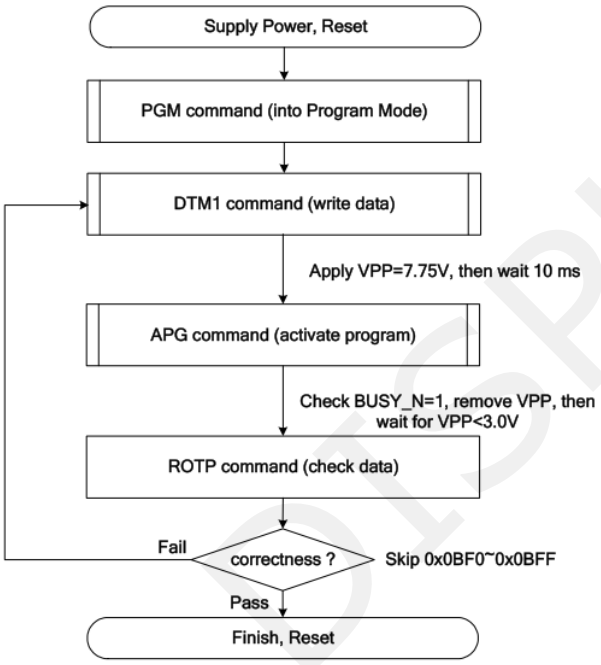
The BUSY_N flag would fall to 0 until the programming is completed.

(45) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



The sequence of programming OTP.

(46) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS_SET[7:0] registers.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

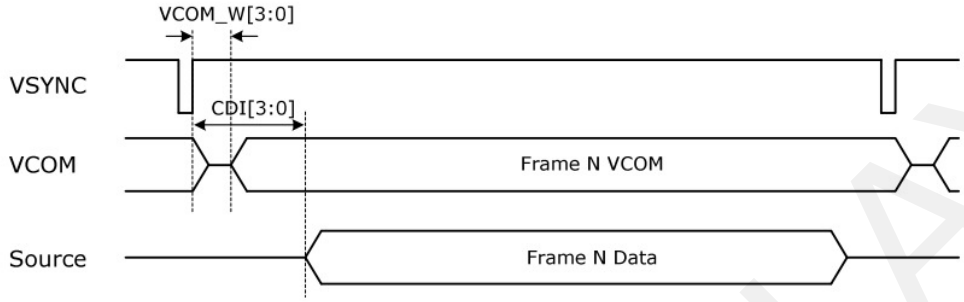
1: Output clock at CL pin to slave chip.

(47) POWER SAVING (PWS) (RE3H)

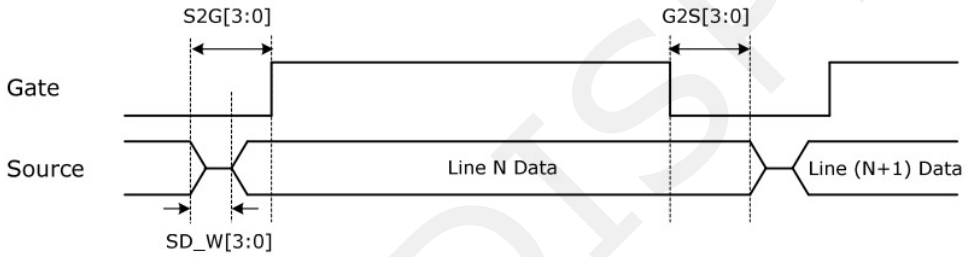
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (Unit: line period)



SD_W[3:0]: Source power saving width (Unit: 660nS)



(48) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(49) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

(50) TEMPERATURE BOUNDARY PHASE-C2 (TSBDRY) (RE7H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Boundary Phase-C2	0	0	1	1	1	0	0	1	1	1	E7h
	0	1	TSBDRY_PHC2[7:0]								00h

This command is used to set the temperature boundary to judge whether booster phase-C2 is applied or not.

8.Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		3	-	sec	
Life		Topr		1000000times or 5years			

Notes:
8-1. Luminance meter: Eye-One Pro Spectrophotometer.
8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.
8-3 WS: White state, DS: Dark state

9.Handling, Safety and Environment Requirements

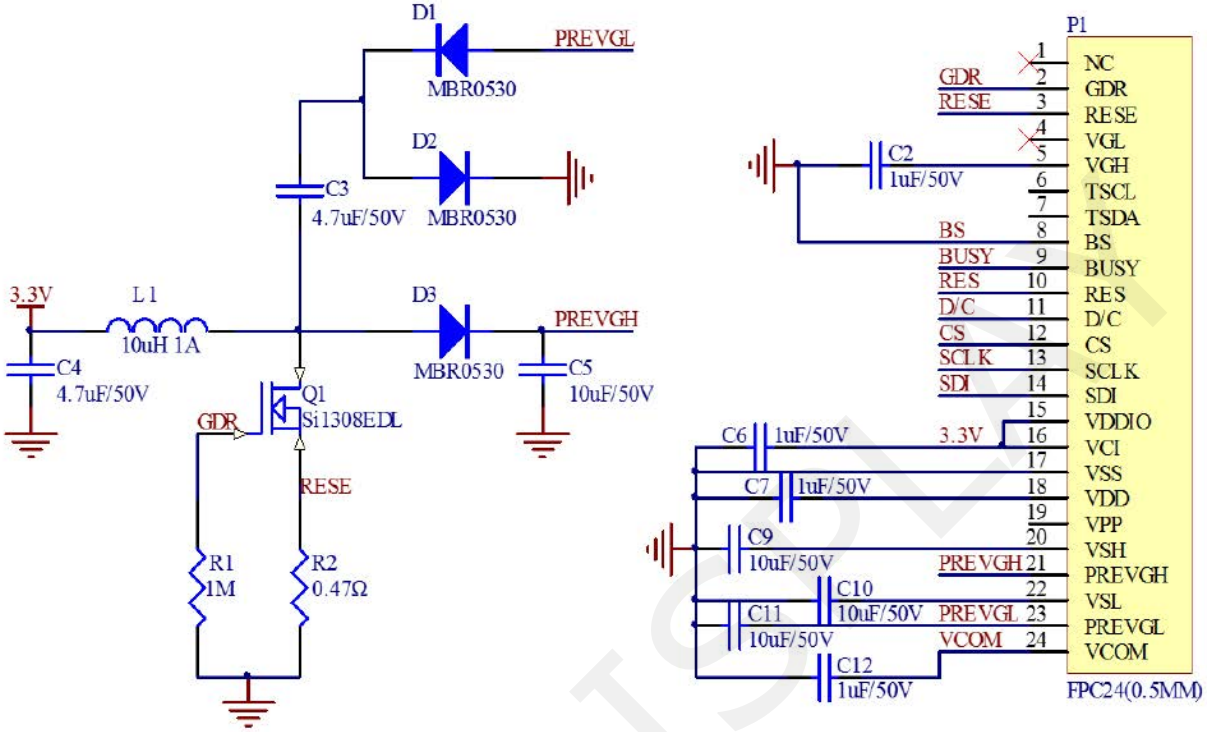
Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module. Disassembling the display module can cause permanent damage and invalidates the warranty agreements. Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.
Data sheet status
Product specification — This data sheet contains final product specifications.
Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification.

10.Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70° C，RH=40%，240h Test in white pattern
3	High-Temperature Operation	T=50° C，RH=35%，240h
4	Low-Temperature Operation	0° C，240h
5	High-Temperature, High-Humidity Operation	T=40° C，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50° C，RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25° C 30min]→[+70 ° C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note:
Put in normal temperature for 1hour after test finished, display performance is ok.

11. Reference Circuit



12. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display ‘s E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.
DESPI Development Kit consists of the development board and the pinboard.

More details about the Development Kit, please click to the following link:

https://www.good-display.com/product/53/

13. Inspection condition

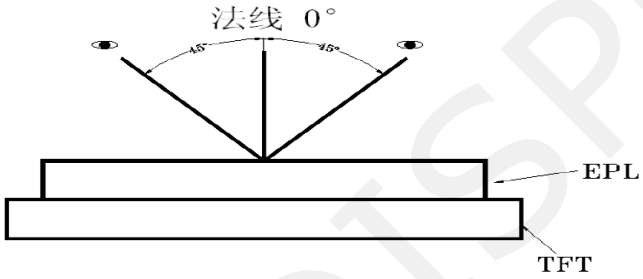
13. 1 Environment

Temperature： 25±3℃
Humidity： 55±10%RH

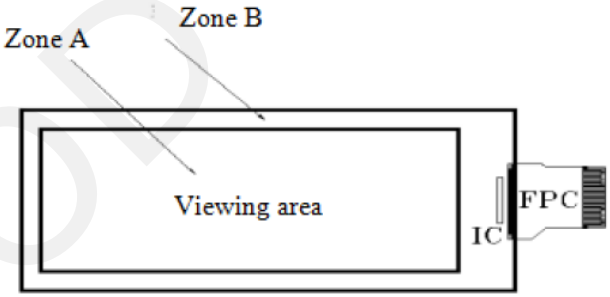
13. 2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

13.3 Inspection method



13. 4 Display area



13. 5 Point and line standard

Name	Causes	Spot size		Part-A	Part-B
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.25mm		Ignore	Ignore
		0.25mm < D ≤ 0.4mm		4	
		0.4mm < D ≤ 0.5mm		2	
		0.5mm < D		0	
Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length	Width	Part-A	Ignore
		L ≤3.0mm	W≤0.1 mm	Ignore	
		3.0 mm < L≤ 6.0mm	0.1 mm<W≤ 0.2mm	2	
		6.0 mm < L	0.2mm < W	0	
Air bubble	Air bubble	D1, D2 ≤ 0.3 mm		Ignore	Ignore
		0.3 mm < D1,D2 ≤ 0.5mm		4	
		0.5mm < D1, D2		0	
Side Fragment					
	X≤6mm, Y≤1mm & display is ok, Ignore				

Remarks: Spot define: That only can be seen under WS or DS defects.

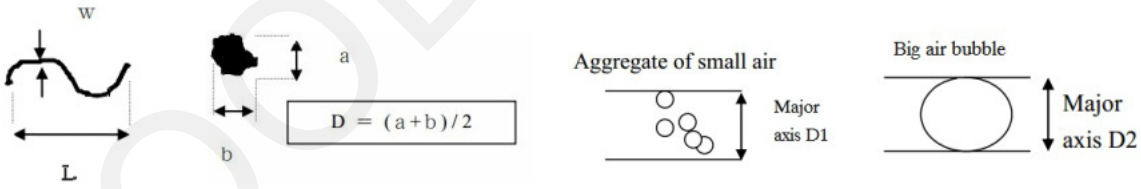
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the "Spot" and "Scratch or line defect".

Spot: W > 1/4L Scratch or line defect: W ≤1/4L

Definition for L/W and D (major axis)

FPC bonding area pad doesn't allowed visual inspection.

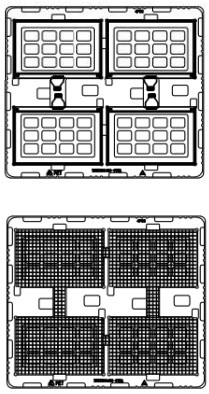


14. Packing

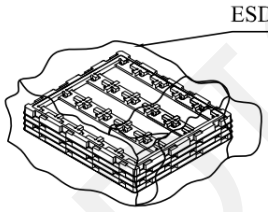
CUSTOMER'S APPROVED:		PAGE: 1/1

PACKLING ORDER:

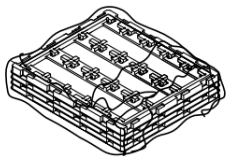
1) Putting 4 pcs Modules on each PET tray.And cover a dedicated EPE film.



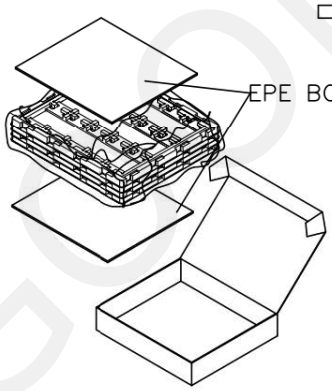
2) Putting 10 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.



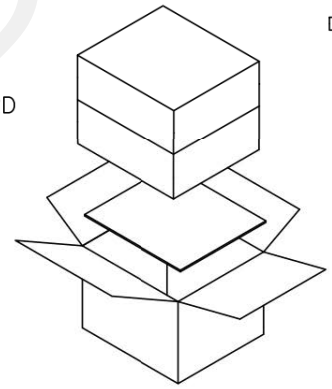
3) the tray together with rubber band



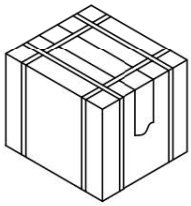
4) Putting in the inner small carton



5) Putting 2 small cartons into one outcarton



6) Packing finished



Note:4 pcs in a tray, 10 trays in a inner carton, 2 inner cartons in a out carton, so 4x10x2=80pcs/Outcarton

Dimension (Small carton): 410*353*112mm Dimension (Out carton): 424*374*250mm

	Drw:		Chk:		Apv:	

15. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:
https://www.good-display.com/news/80.html