JADARD

JD79667AA

Data Sheet

All-in-one driver with
TCON for Color application

Version 1.0.3
2023/06/20

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 2-bit output per pixel. The timing controller provides control signals for the source driver and gate drivers.

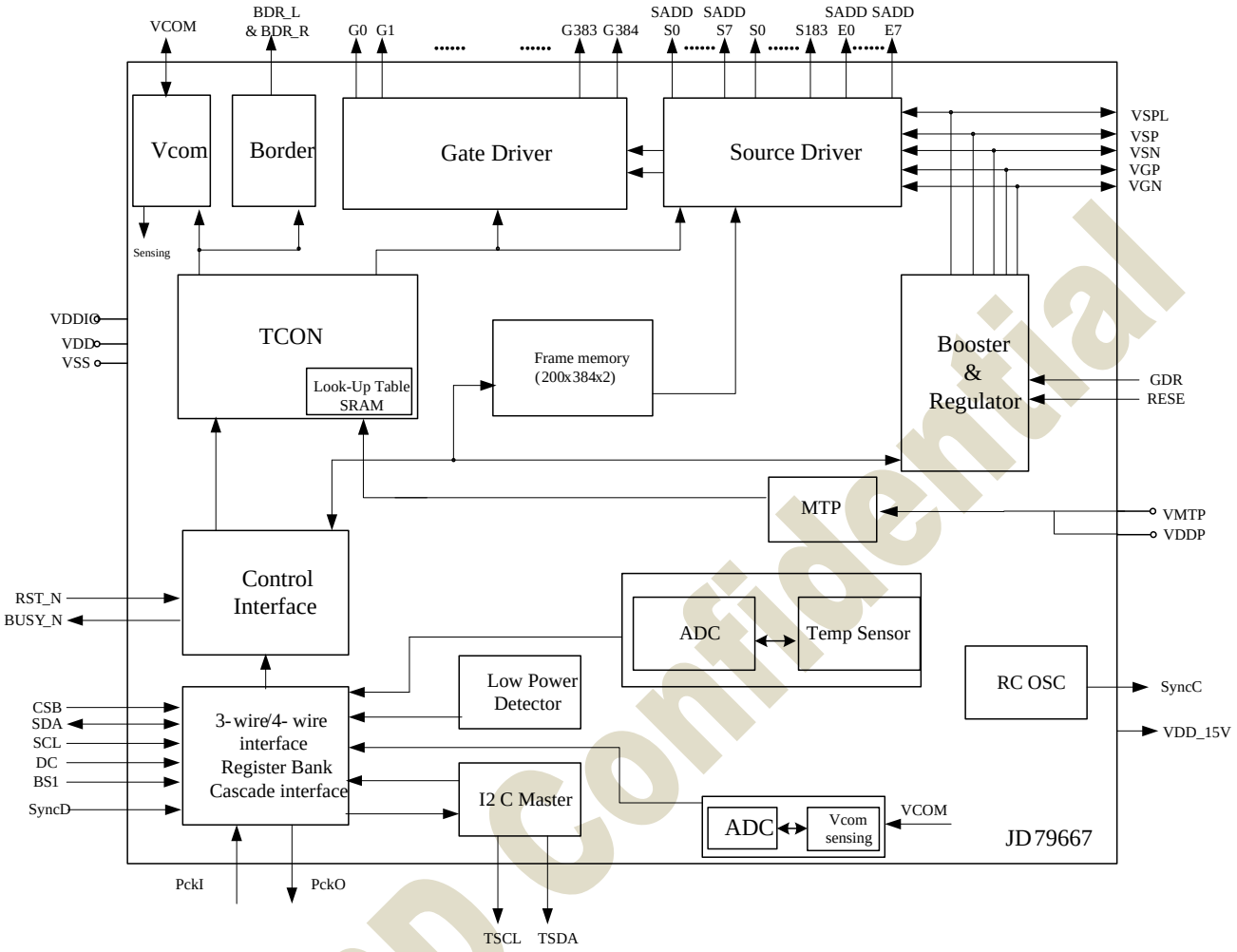
The DC-DC controller allows to generate the source output voltage VSP_0/VSN_0(+/-15V),VSP_1/VSPL_0/VSPL_1/VSN_1 (+/-3V~+/-15V) and VGP/VGN(+/-20V, +/-17V, +/-15V, +/-10V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire(SPI) serial.

2. FEATURES

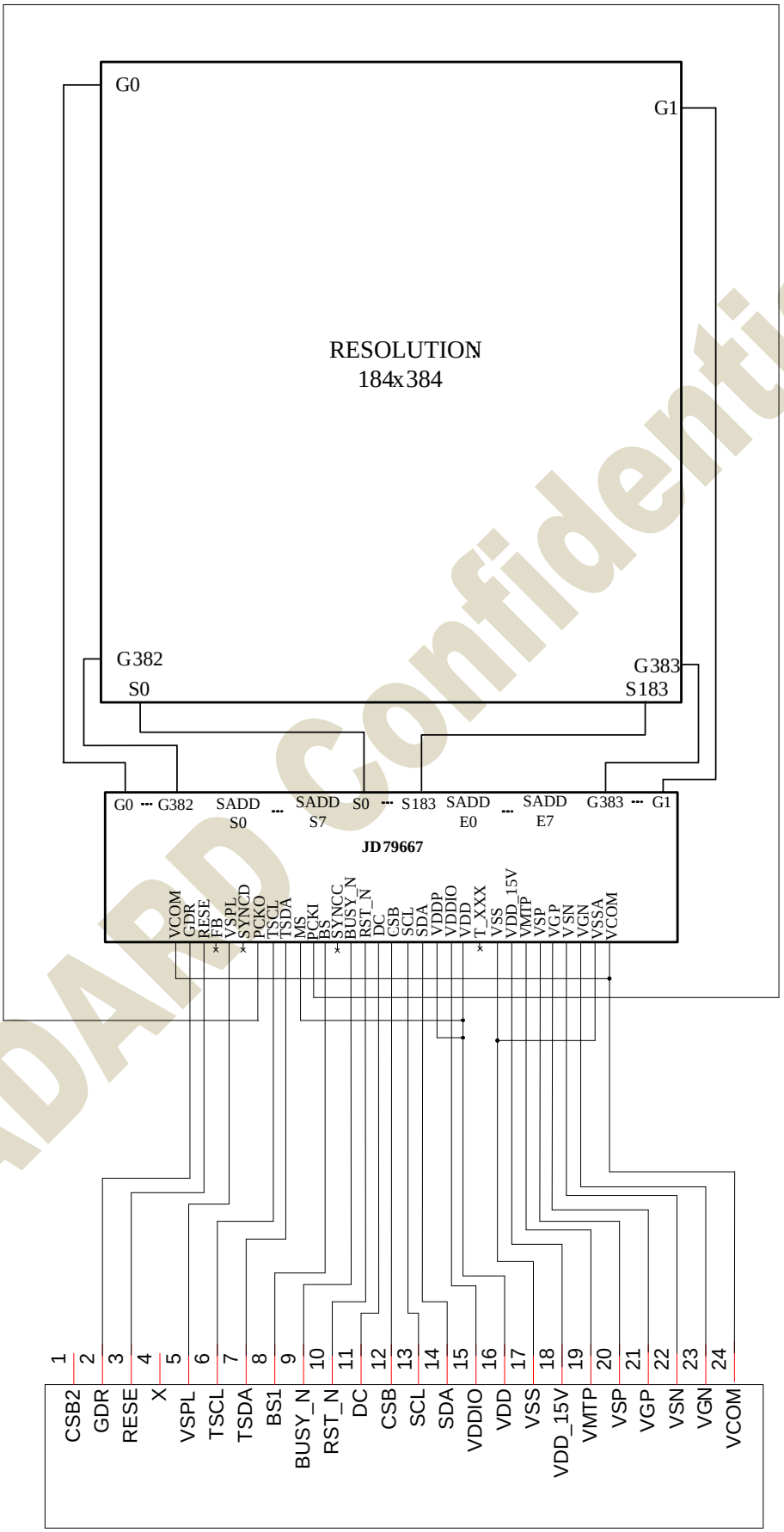
- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 200x384)
- Support source & gate driver function:
  - 200 Outputs source driver with 2-bit black/white/red/yellow per pixel:
    - Output dynamic range(Voltage step:100mV):
      - Mode 0: 0V & VSP_0(+15V) & VSN_0(-15V) & VSPL_0(+3V~+15V)
      - Mode 1: 0V & VSP_1 (+3V ~ +15V) & VSN_1(-3V ~ -15V) & VSPL_1 (+3V ~ +15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 384 Output gate driver:
    - Output dynamic range: VGP and VGN(+/-20V, +/-17V, +/-15V, +/-10V)
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (7-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: 200 x 384 x 2 bit SRAM
- Built in temperature sensor:
  - On-Chip: -25 ^{o}C ~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V

- 6K-byte MTP for LUT, User command
- Partial update
- Support cascade
- Package-COG

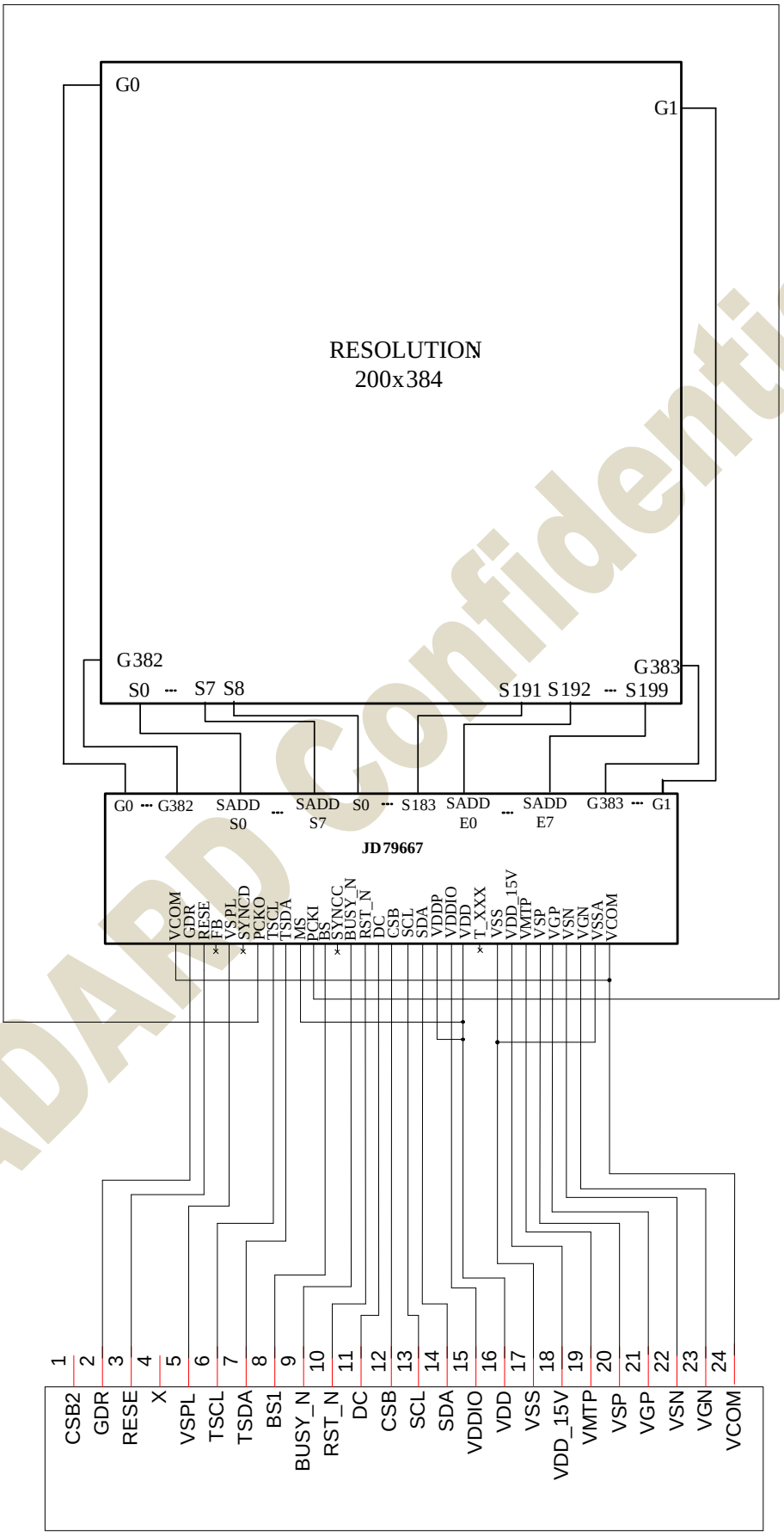
3. BLOCK DIAGRAM



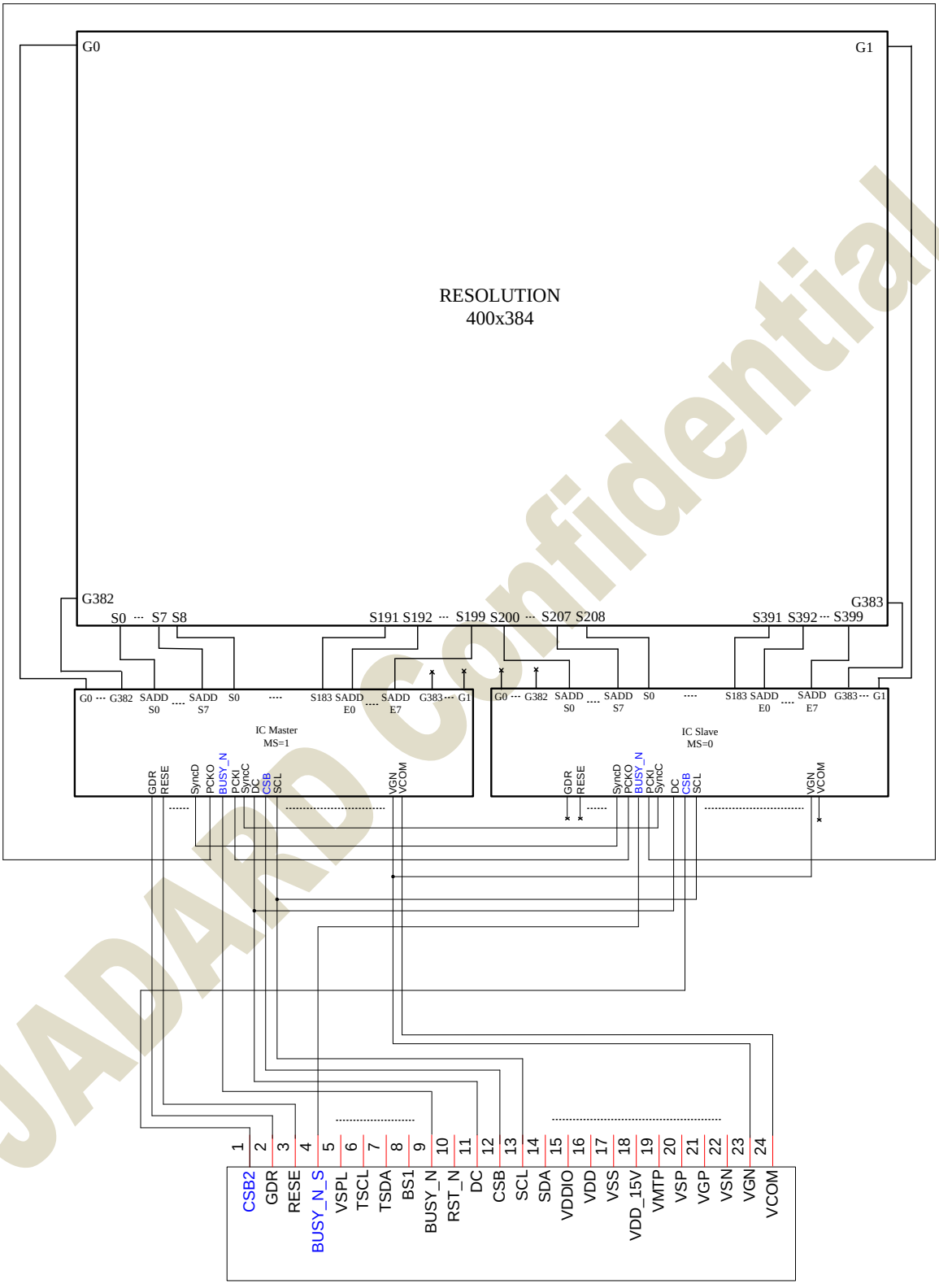
Normal type 1 (source resolution below 184ch.)



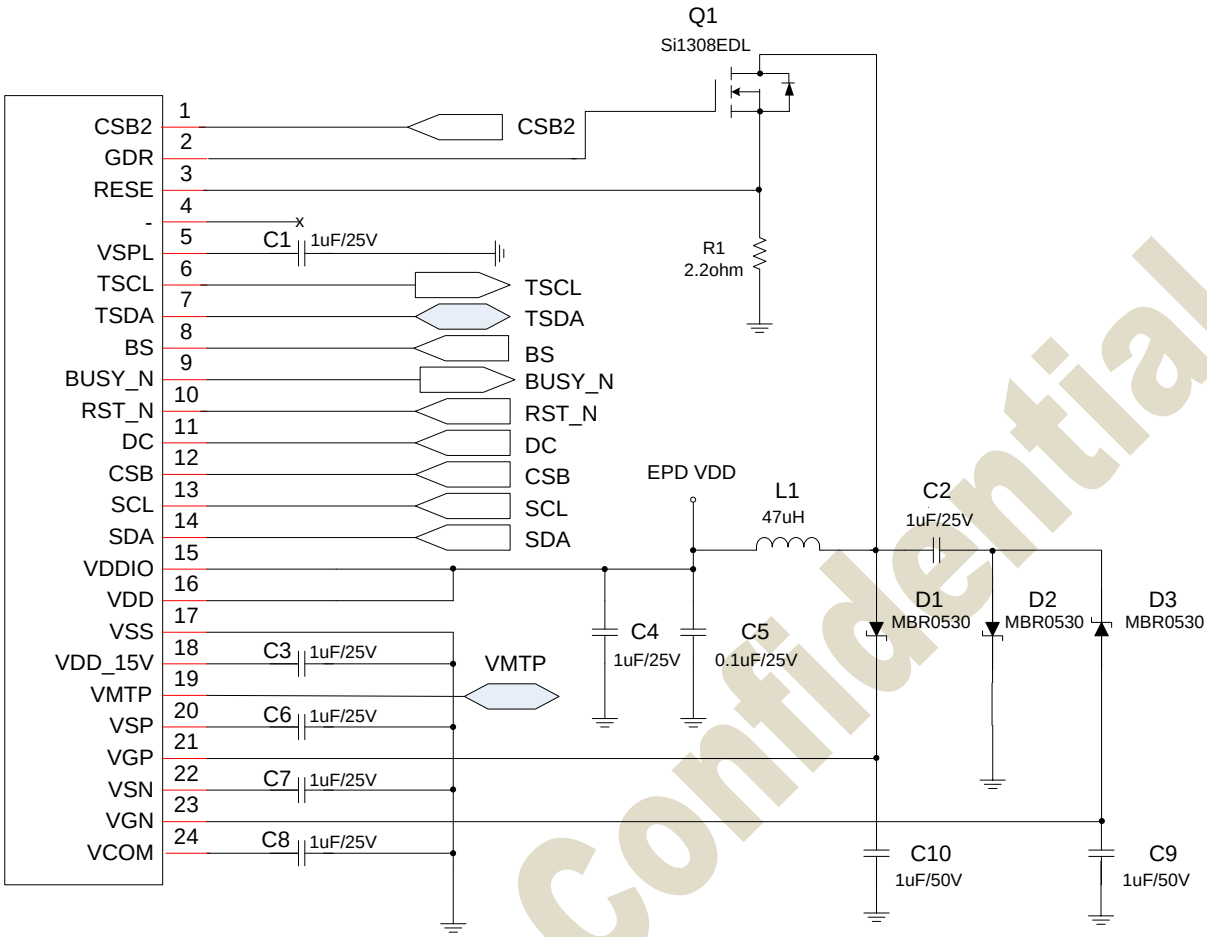
Normal type 2 (source resolution 200ch.)

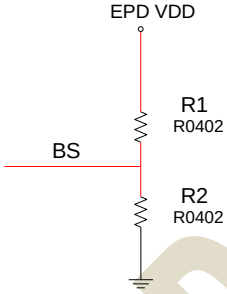


Cascade type

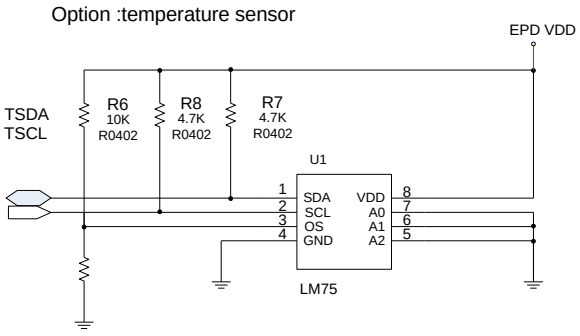


4. APPLICATION CIRCUIT





	R1	R2
3- wire SPI (CSB, SDA, SCL)	10K	NC
4-wire SPI (DC, CSB, SDA, SCL)	NC	10K

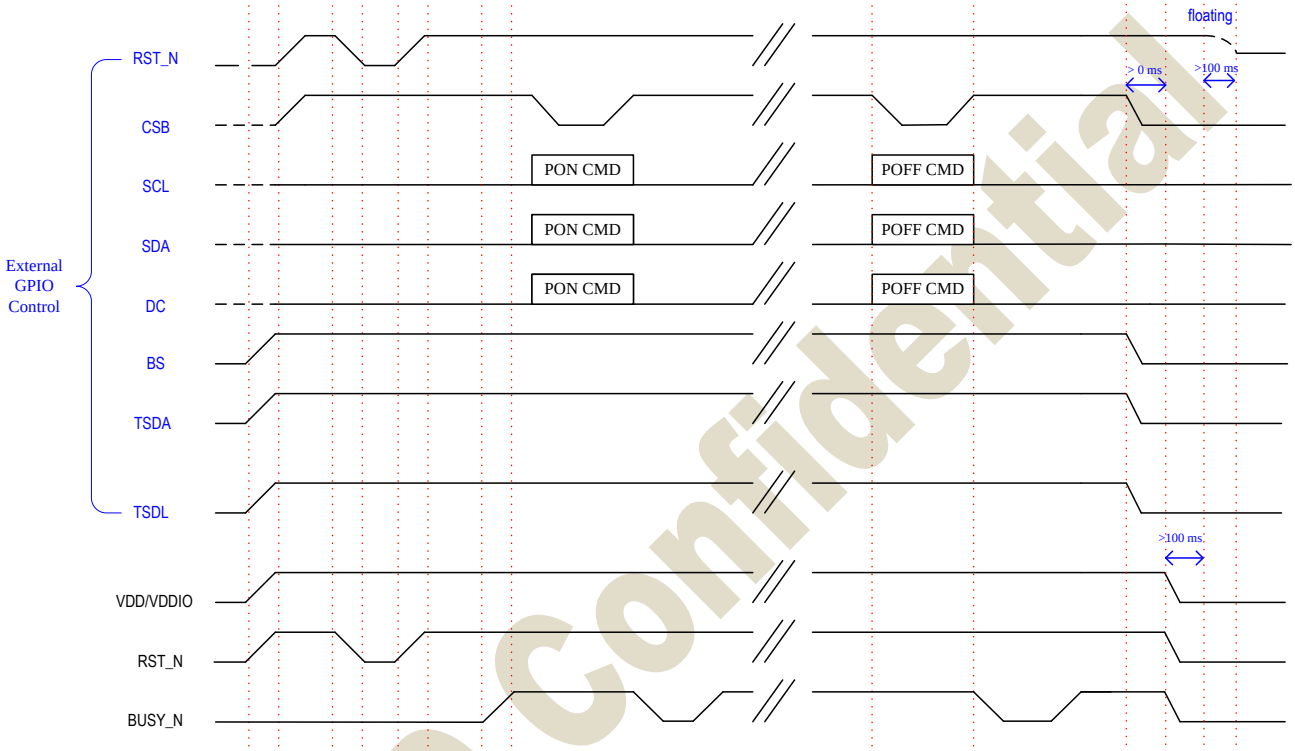


Reference table of the device:

Device no.	Value	Reference
C1,C2,C3, C4, C6, C7, C8	1uF	0603, X5R/X7R, voltage rating : 25V
C9, C10	1uF	0603, X5R/X7R, voltage rating : 50V
C5	0.1uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47uH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ

D1~D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV

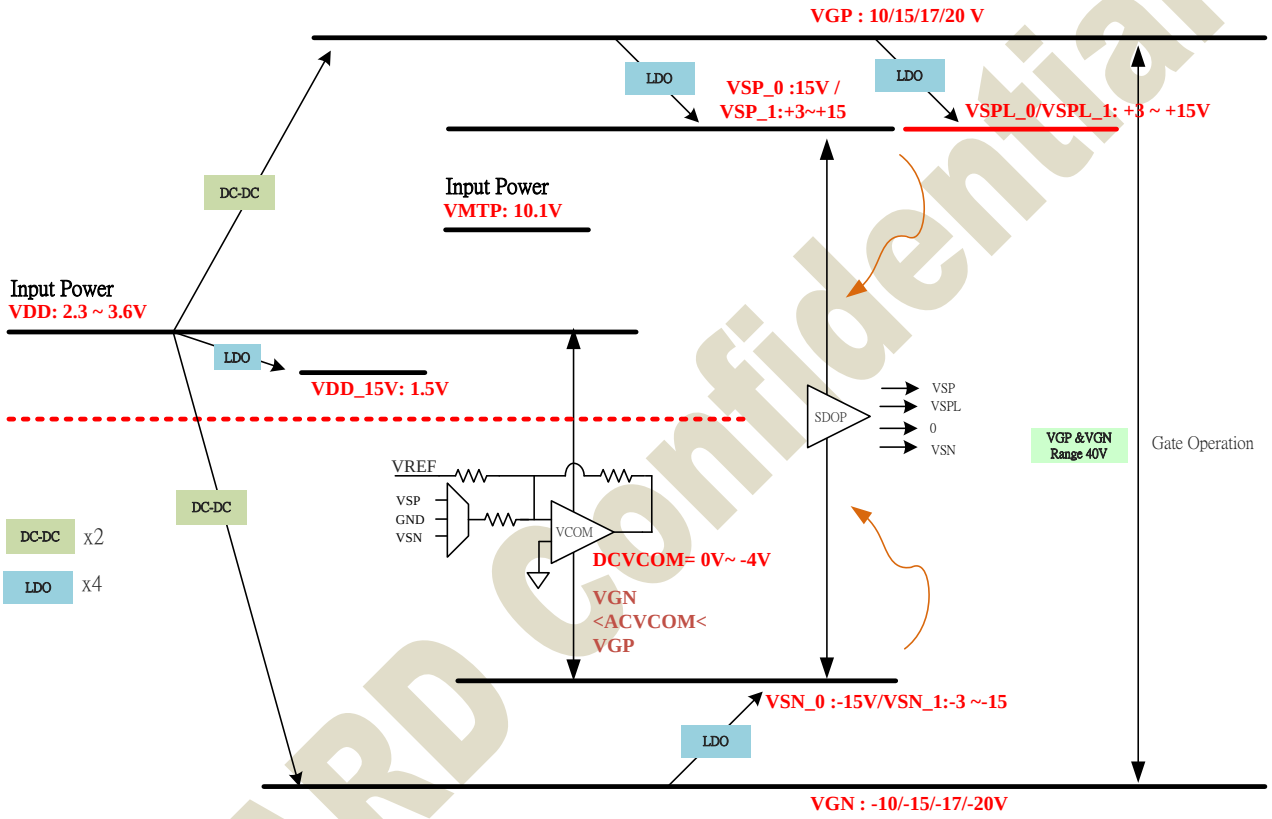
4.1 External GPIO Control



Note:
TSDA: I^{2}C data for external temperature sensor
TSCL: I^{2}C clock for external temperature sensor
(I^{2}C interface need external pull high resistance. Pull low or floating If not used.)

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

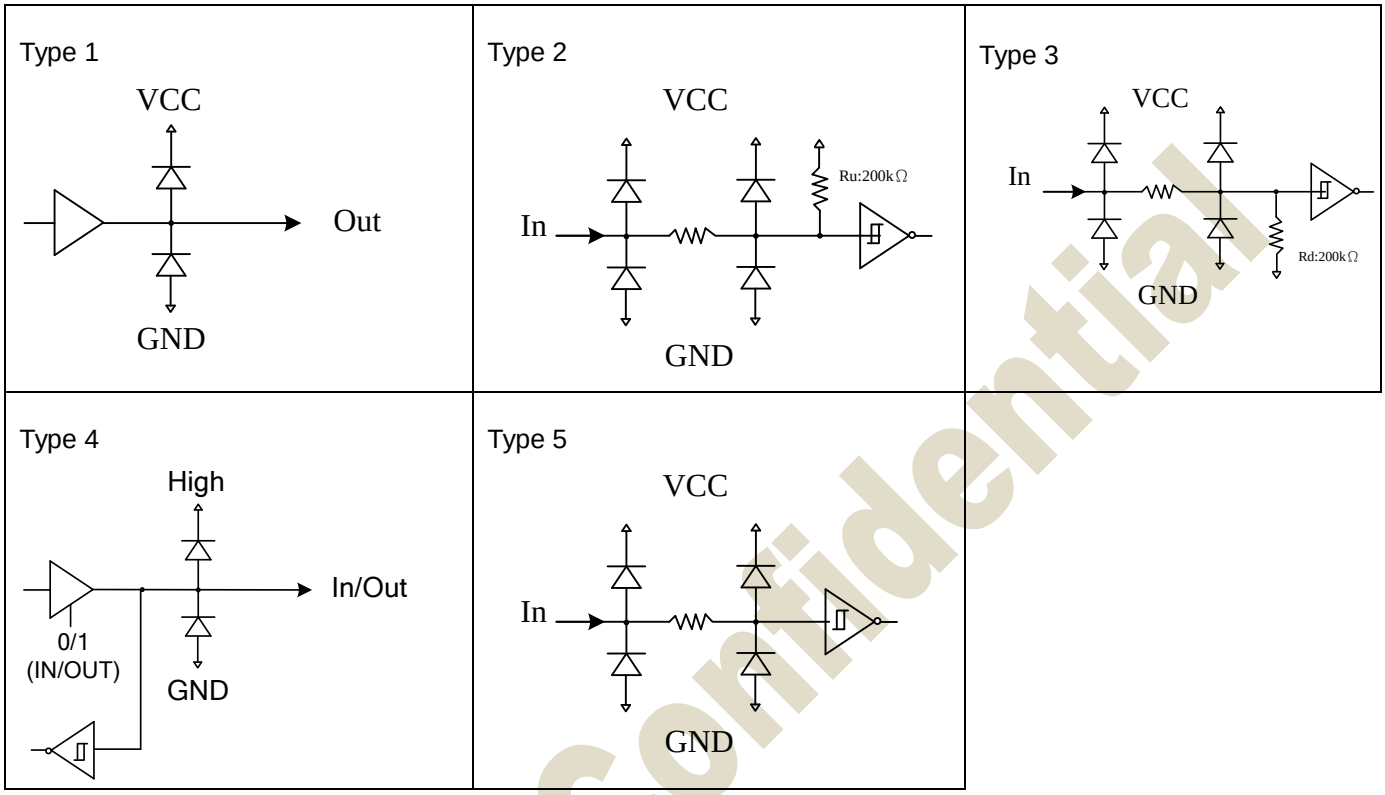
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. (normal pull high) When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF
TSCL	O	Type1	I^2C clock for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.
TSDA	I/O	Type 4	I^2C data for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[183:0]	O	-	Source driver output signals.
S_ADDS/E[7:0]	O	-	Source driver output signals.
G[383:0]	O	-	Gate driver output signals..
Border			
VBD[4:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) V 2. (15 +(- VCM_DC)) V or (-15 +(- VCM_DC)) V 3. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGP	P	Type 5	Positive gate voltage

Pin Name	Pin Type	I/O Structure	Description
VGN	P	Type 4	Negative gate voltage.
VSP	P	Type 1	Positive source voltage
VSN	P	Type 1	Negative source voltage.
VSPL	P	Type 1	Positive source voltage
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_15V	P	-	1.5V voltage input &output
VMTP	P	-	MTP program power (10.1V)
Reserved Pins			
TP [21:0]	I/O	-	Test pin.Leave open or pull gnd if it is not used.
SyncD	I/O	Type 4	Cascade data signal. Leave open or pull gnd if it is not used.
SyncC	I/O	Type 4	Cascade clock signal. Leave open or pull gnd if it is not used.
PckI	I	Type 3	Break panel check input. Leave open or gnd if it is not used.
PckO	O	Type 1	Break panel check output. Leave open or gnd if it is not used.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGP	5ohm	TSCL	100ohm
VGN	5ohm	BUSY_N	100ohm
VSP	5ohm	BS	100ohm
VSN	5ohm	RESE	5ohm
VSPL	5ohm	GDR	5ohm
VMTP	5ohm	SDA	100ohm
VDD_18V	5ohm	SCL	100ohm
VSSA	5ohm	CSB	100ohm
VDDIO	5ohm	DC	100ohm
VSS	5ohm	RST_N	100ohm
VDDP	5ohm	SyncD	100ohm
VDD	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
TP [21:0]	100ohm	PCKO	100ohm

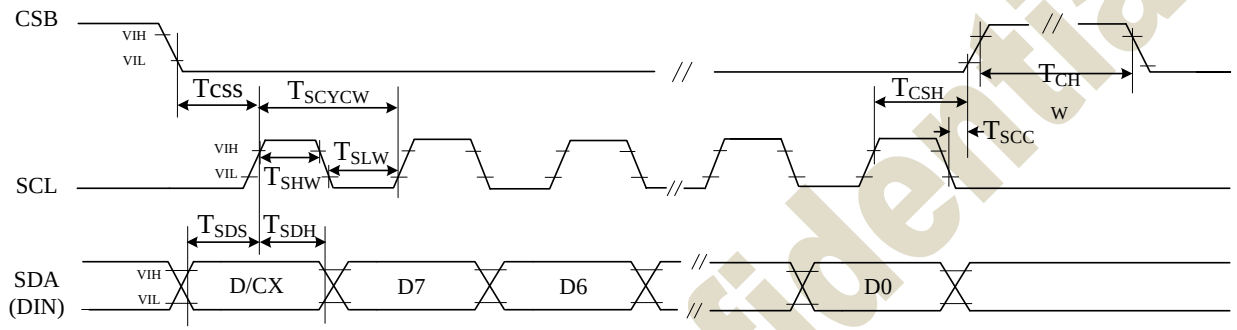
7. SPI COMMAND DESCRIPTION

JD79667 use the 3-wire/4-wire serial port as communication interface for all the function and command setting.

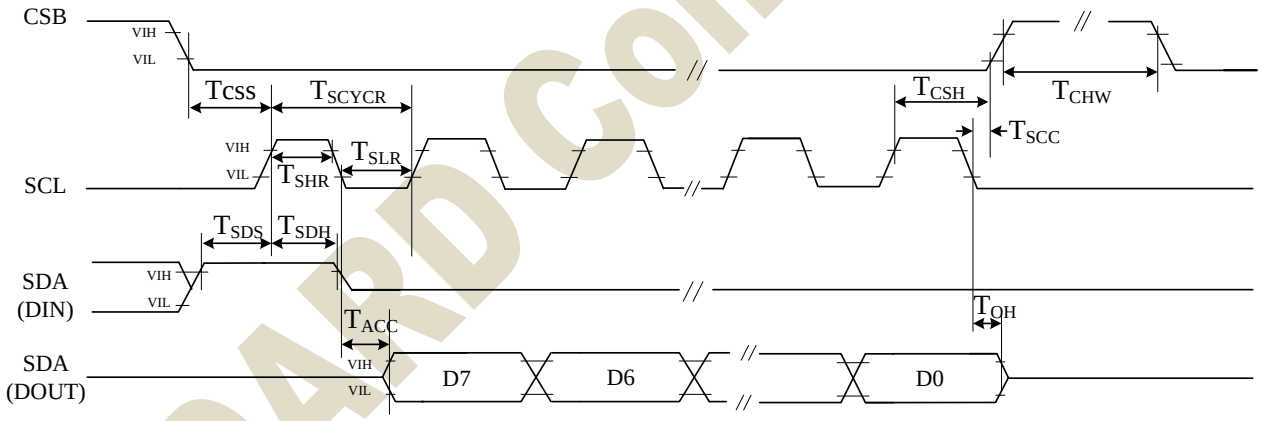
JD79667 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

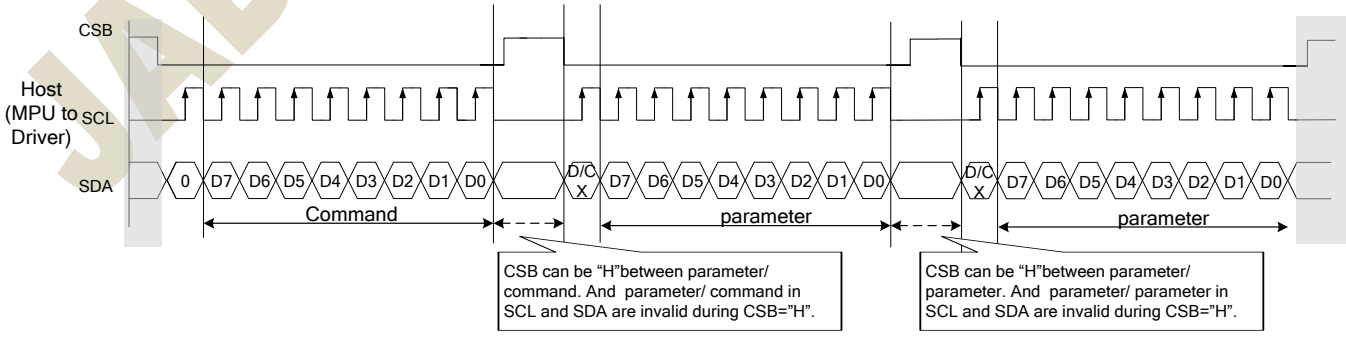
7.1 “3-Wire” Serial Port Interface



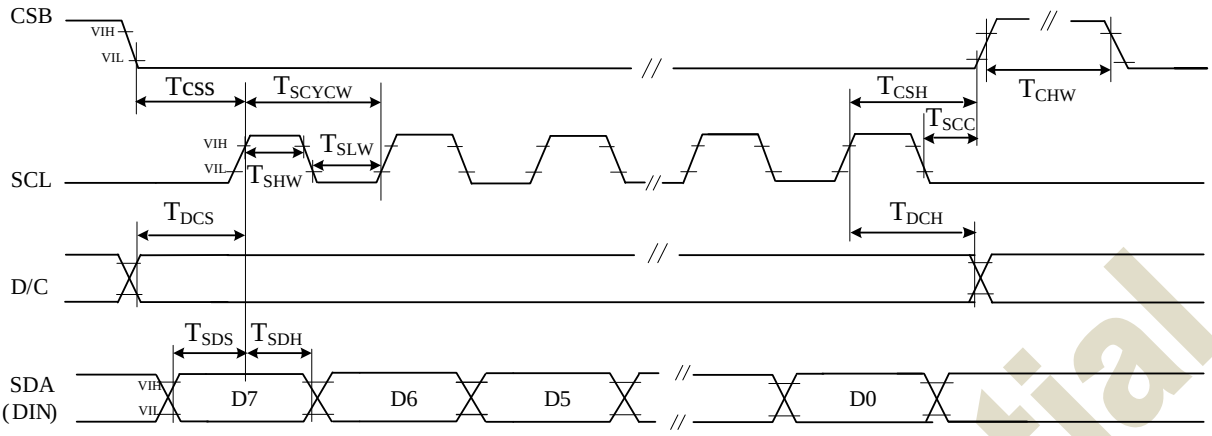
3 pin serial interface characteristics (write mode)



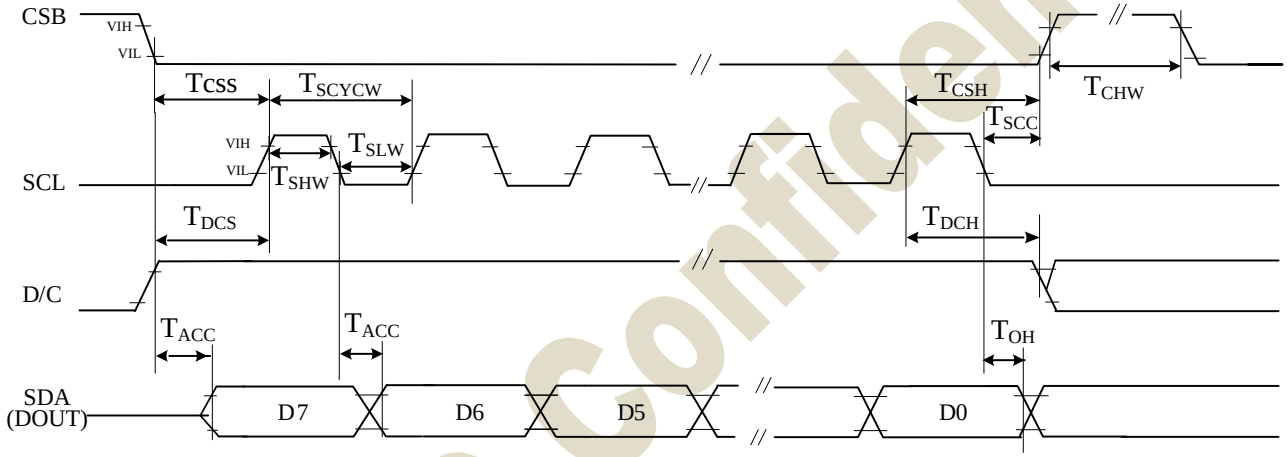
3 pin serial interface characteristics (read mode)



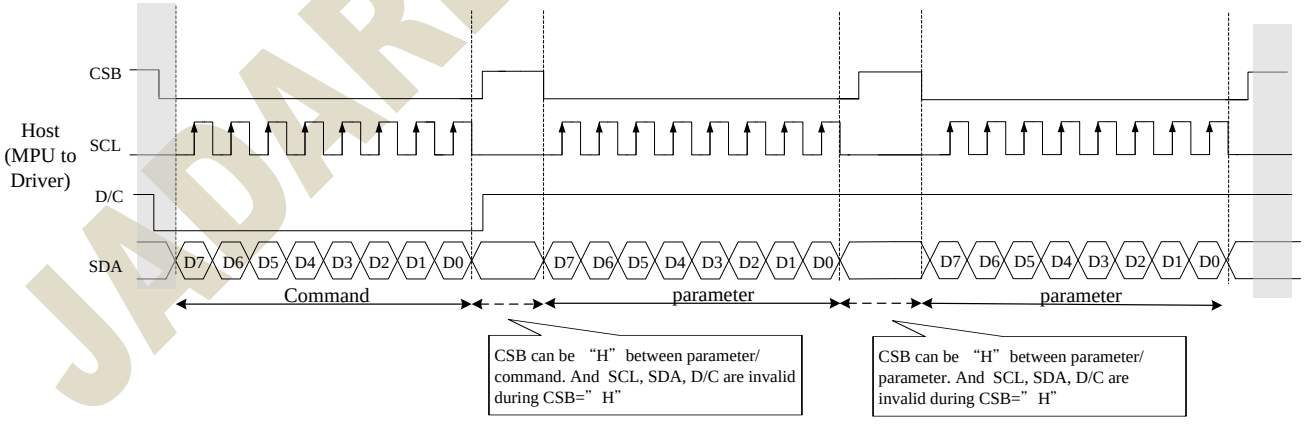
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79667. Refer to the next section for detail register function description.

Address	command			Bit								
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	PHA_ON[5:0]						02h
		W	1	-	-	PHA_OFF[5:0]						07h
		W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	00H
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna		FR[2:0]		02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/ TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(8)	VRES(0)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	-	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	0	0	1	1	05h
		R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	01h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	-	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMOD	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
R9FH	Read MTP Reserved Bytes(RMRB)	W	0	1	0	0	1	1	1	1	1	9FH
		R	1	#	#	#	#	#	#	#	#	-
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h
		R	1	Chk_CRC[7:0]								00h
		R	1	MTP_CRC[7:0]								00h

8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1 R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source/Boder/Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 200x384 (default) 01: Display resolution is 184x384 10: Display resolution is 168x384 11: Display resolution is 200x200

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display,the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction	

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)
3	V_MODE	Source Power switching mode. 0: Mode0(default) 1: Mode1

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	**Internal VSP & VSPL power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	**Internal VSN power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
   I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	10v	+10v
	VGN	10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)
	VCOMDC	-2v	-2v

4. Voltage setting limit: VSP_0 ≥ VSPL_0 , VSP_1 ≥ VSPL_1

Restriction	

8.2.3R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R02h = 0x00h ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.2.4 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence(base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.2.5 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
	000001	Period2	010111	Period24	101101	Period46
	000010	Period3	011000	Period25	101110	Period47
	000011	Period4	011001	Period26	101111	Period48
	000100	Period5	011010	Period27	110000	Period49
	000101	Period6	011011	Period28	110001	Period50
	000110	Period7	011100	Period29	110010	Period51
	000111	Period8	011101	Period30	110011	Period52
	001000	Period9	011110	Period31	110100	Period53
	001001	Period10	011111	Period32	110101	Period54
	001010	Period11	100000	Period33	110110	Period55
	001011	Period12	100001	Period34	110111	Period56
	001100	Period13	100010	Period35	111000	Period57
	001101	Period14	100011	Period36	111001	Period58
	001110	Period15	100100	Period37	111010	Period59
	001111	Period16	100101	Period38	111011	Period60
	010000	Period17	100110	Period39	111100	Period61
	010001	Period18	100111	Period40	111101	Period62
	010010	Period19	101000	Period41	111110	Period63
	010011	Period20	101001	Period42	111111	Period64
	010100	Period21	101010	Period43		
	010101	Period22	101011	Period44		

Restriction

8.2.6 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.2.7 R10H (DTM): Data Start transmission Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM	W	0	0	0	0	1	0	0	0	0	10H
2 bit mode	W	1									
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
:	W	1	:		:		:		:		00h
Mth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.

Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1,Pixel[1:0]=01 ->Gray level select=Gray1,follow LUT data output from IP output port"ogray01".

When DDX=0,Pixel[1:0]=11 ->Gray level select=Gray0,follow LUT data output from IP output port"ogray00"

Restriction

8.2.8 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / Data_flag / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.2.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R12H=0x00 While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

8.2.10 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

8.2.13 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

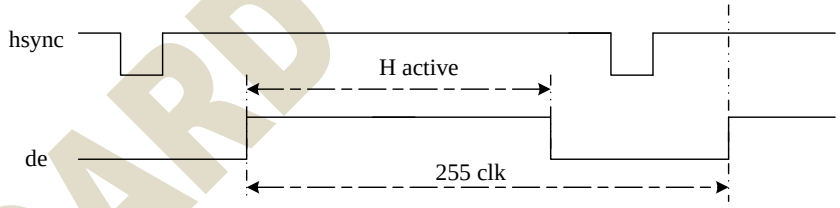
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

bit3	Dynamic frame rate
0	Disable(default)
1	Enable

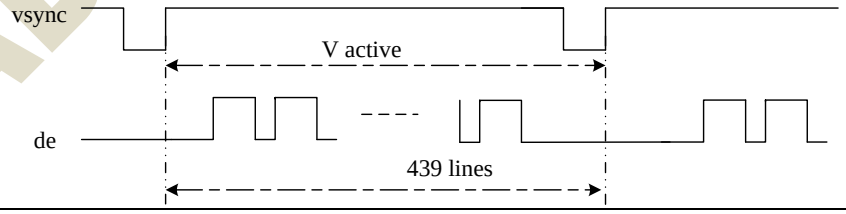
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



Restriction

8.2.14 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

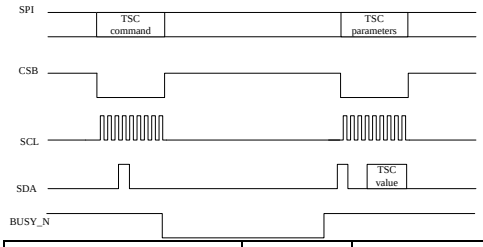
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[9:8]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

8.2.15 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +0.5℃ 0010: +1℃ 0011: +1.5℃ 0100: +2℃ 0101: +2.5℃ 0110: +3℃ 0111: +3.5℃ 1000: -4℃ 1001: -3.5℃ 1010: -3℃ 1011: -2.5℃ 1100: -2℃ 1101: -1.5℃ 1110: -1℃ 1111: -0.5℃
4	TO[4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

8.2.16 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	**I**2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction: This command only actives after R04H(PON)

8.2.17 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

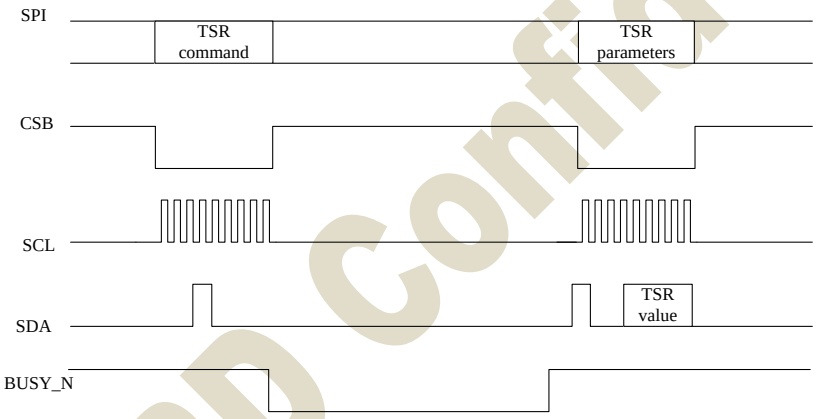
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction: This command only actives after R04H(PON)

8.2.18 R50H (CDI): VCOM and DATA interval setting Register

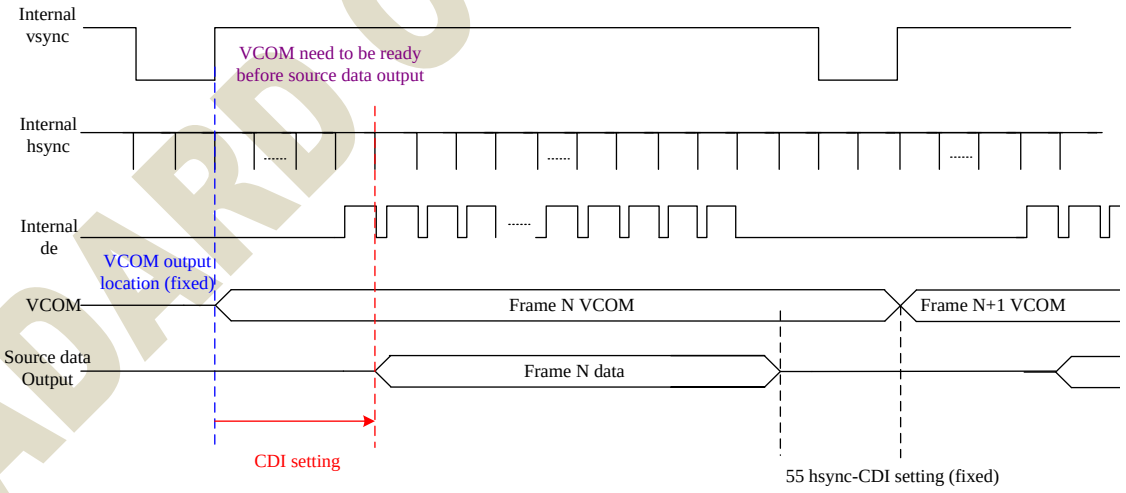
R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)
:
CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.

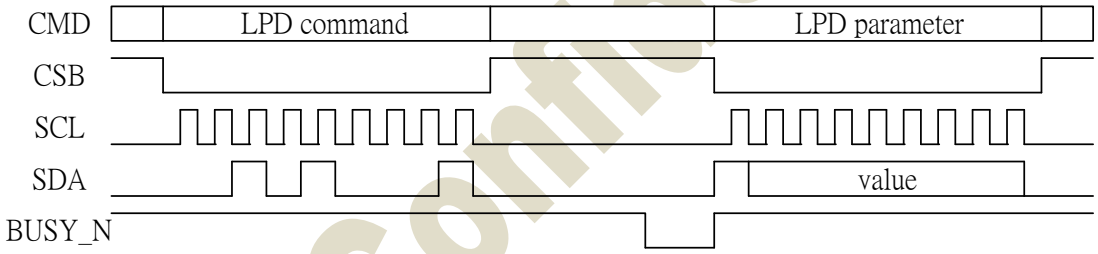
Boarder output will follow FOPT definition being defined in R00h.

Restriction	

8.2.19 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)). 1st Parameter: Bit 0 = LPD 0 = Low power input. 1 = Normal status. 
Restriction	This command only actives when BUSY_N = "1".

8.2.20 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3th Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Note: No matter HRES[9:8],HRES[1:0],VRST[9] value being filled, it's always be 00b. Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1 EX :200X384 GD: First G active = G0 LAST active GD= 0+384-1= 383; (G383) SD : First active channel: =S0 LAST active SD=0+50*4-1=199; (S199) Note : Only supports source 200.ch for source 184ch. above
Restriction	Horizontal resolution should be 4-multiple.

8.2.21 R65H(GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3rd Parameter	W	1	-	-	-	-	-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Note: No matter S_start[9:8], S_start [1:0],VRST[9] value being filled, it's always be 00b. 1.S_Start [7:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line
Restriction	S_Start should be the multiple of 4

8.2.22 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	0	0	0	0	0	0	1	1	05h
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st & 2nd & 3rd Parameter:

Bit	Description
7-0	CHIP_REV

Restriction	

8.2.23 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

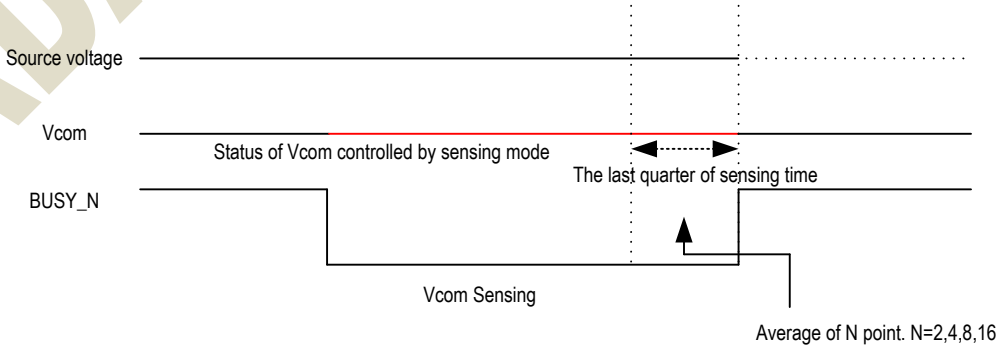
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s
7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16



Restriction: This command only actives when BUSY_N = "1".

8.2.24 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
6-0	VV[6:0]	VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

8.2.25 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit	Name	Description
6-0	VDCS[6:0]	VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

	7	MTP_VCM	Follow MTP VCOM value in MTP mode 0: From the setting of MTP (default) 1:From the setting of register
Restriction			

8.2.26 R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	-	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode

Note:
No matter HRST[1:0] ,HRST[9:8],HRED[9:8],VRST[9],VRED[9] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

Gates scan both inside and outside of the partial window.

Restriction

8.2.27 R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

8.2.28 R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.29 R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the MTP								-

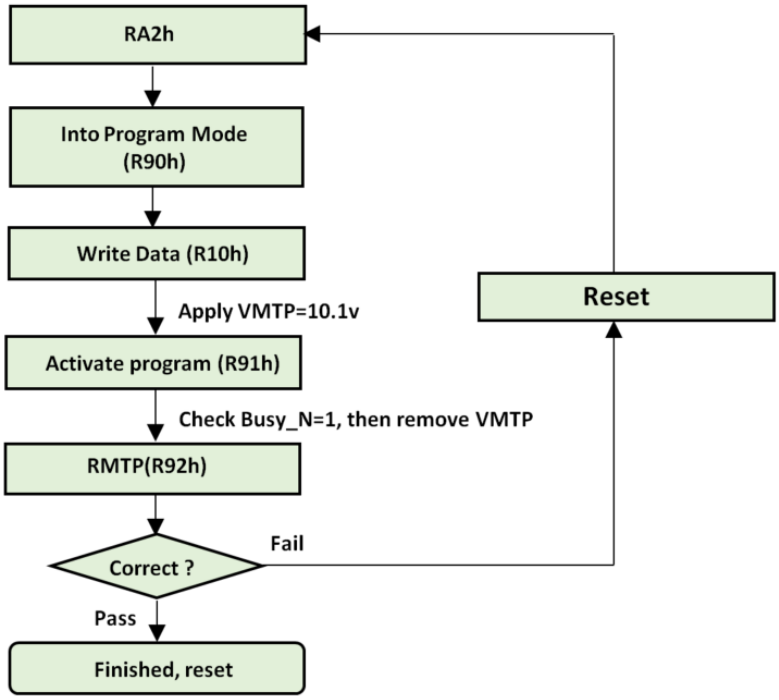
NOTE: "-" Don't care, can be set to VDD or GND level

Description

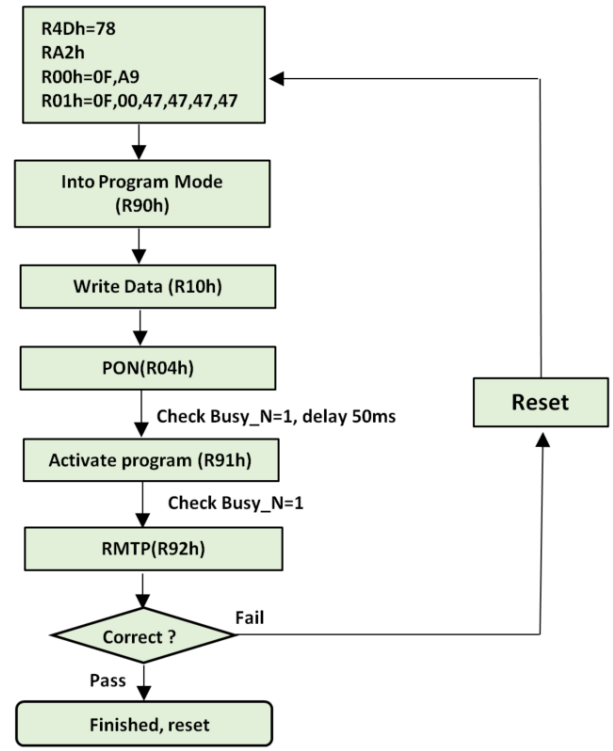
-The command define as follows:

The command is used for reading the content of MTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF



The sequence of programming MTP(External power)



The sequence of programming MTP(Internal power)

Restriction	This command only actives when BUSY_N = “1”.

8.2.30 R9FH(RMRB) Read MTP Reserved Bytes

R9FH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMRB	W	0	1	0	0	1	1	1	1	1	9FH
1st Parameter	R	1	Dummy								00h
2nd Parameter	R	1	The data of address 0x16F7 in the MTP								00h
3rd Parameter	R	1	:								00h
:	R	1	:								00h
97th Parameter	R	1	:								00h
98th Parameter	R	1	:								00h
101th Parameter	R	1	The data of address 0x175A in the MTP								00h

Description	-The command define as follows: The command is used for reading the content of MTP Reserved Byte for checking the data of programming. This command could read these information from MTP directly.
Restriction	

8.2.31 RE3H (PWS): Power Saving Register

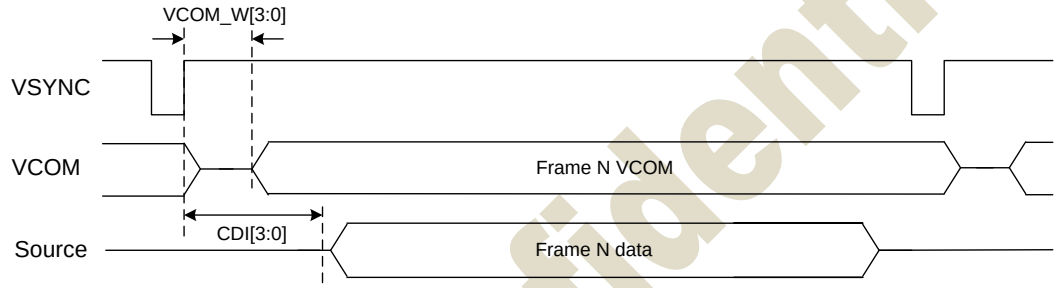
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

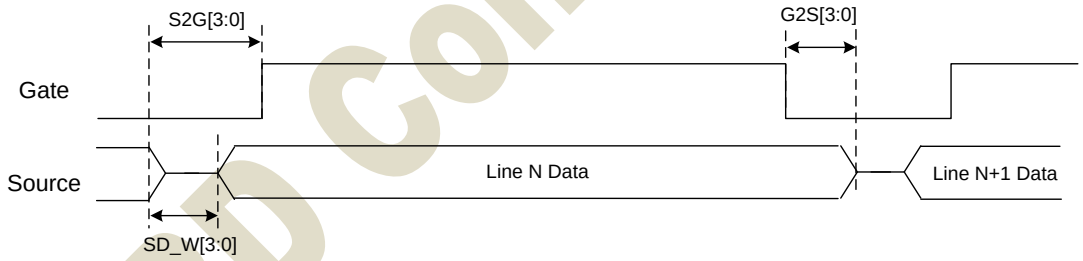
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 500nS), SD_W<=S2G



Restriction

8.2.32 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

Restriction	

Register Restriction

Following table will indicate the register restriction:

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R04H(PON)	X	Flag
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R17H(AUTO)	Valid in standby	Flag
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R61H(TRES)	X	No action
R65H(GSST)	X	No action
R70H(REV)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R83H(PTL)	X	No action
R90H(PGM)	X	No action
R91H(APG)	X	Flag
R92H(RMTP)	X	Flag
R9FH(Read MTP reserved)	Valid only read	Flag
RE3H(PWS)	X	No action
RE4H(LVSEL)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

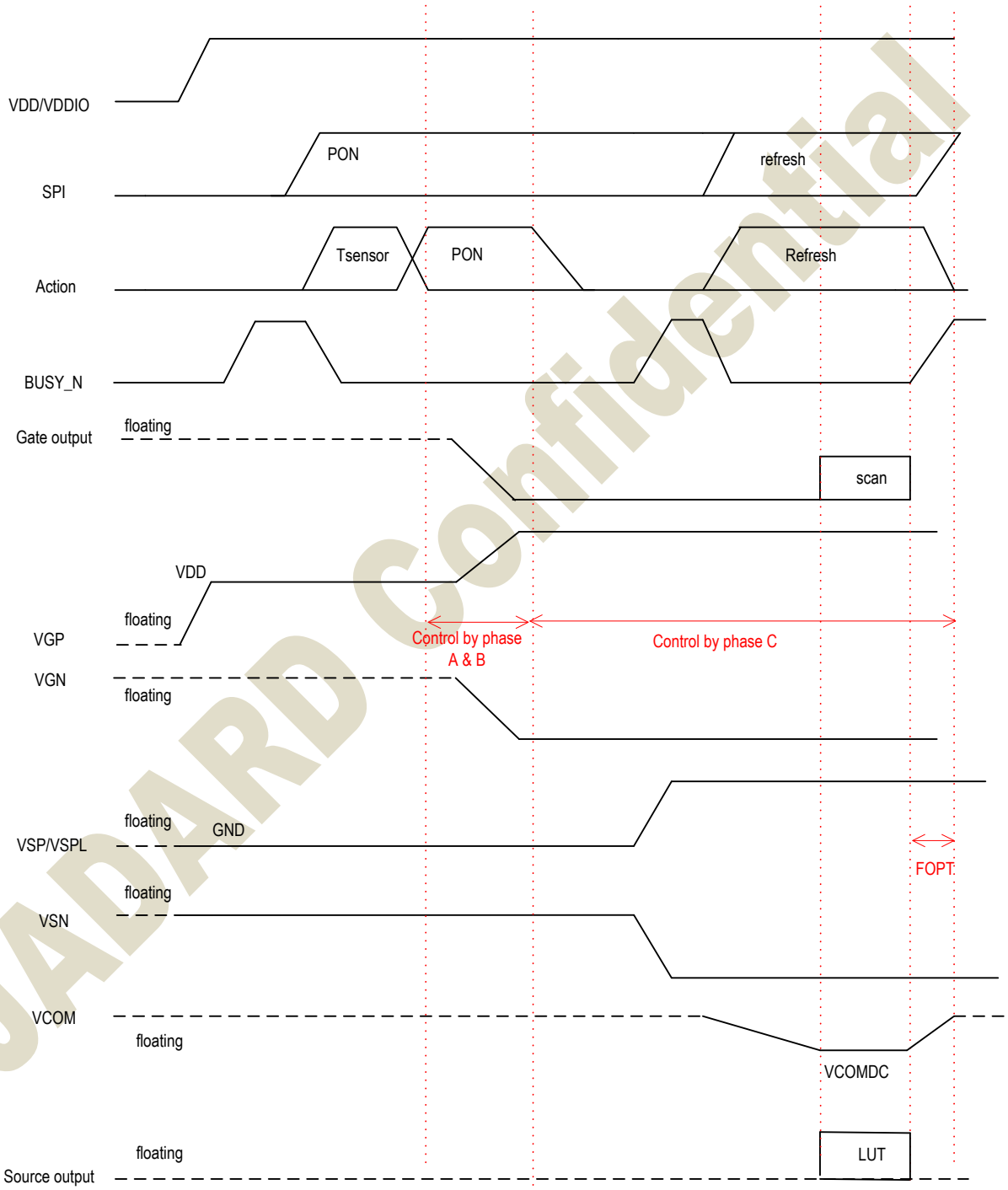


Figure 1: Power on sequence

Power off Sequence

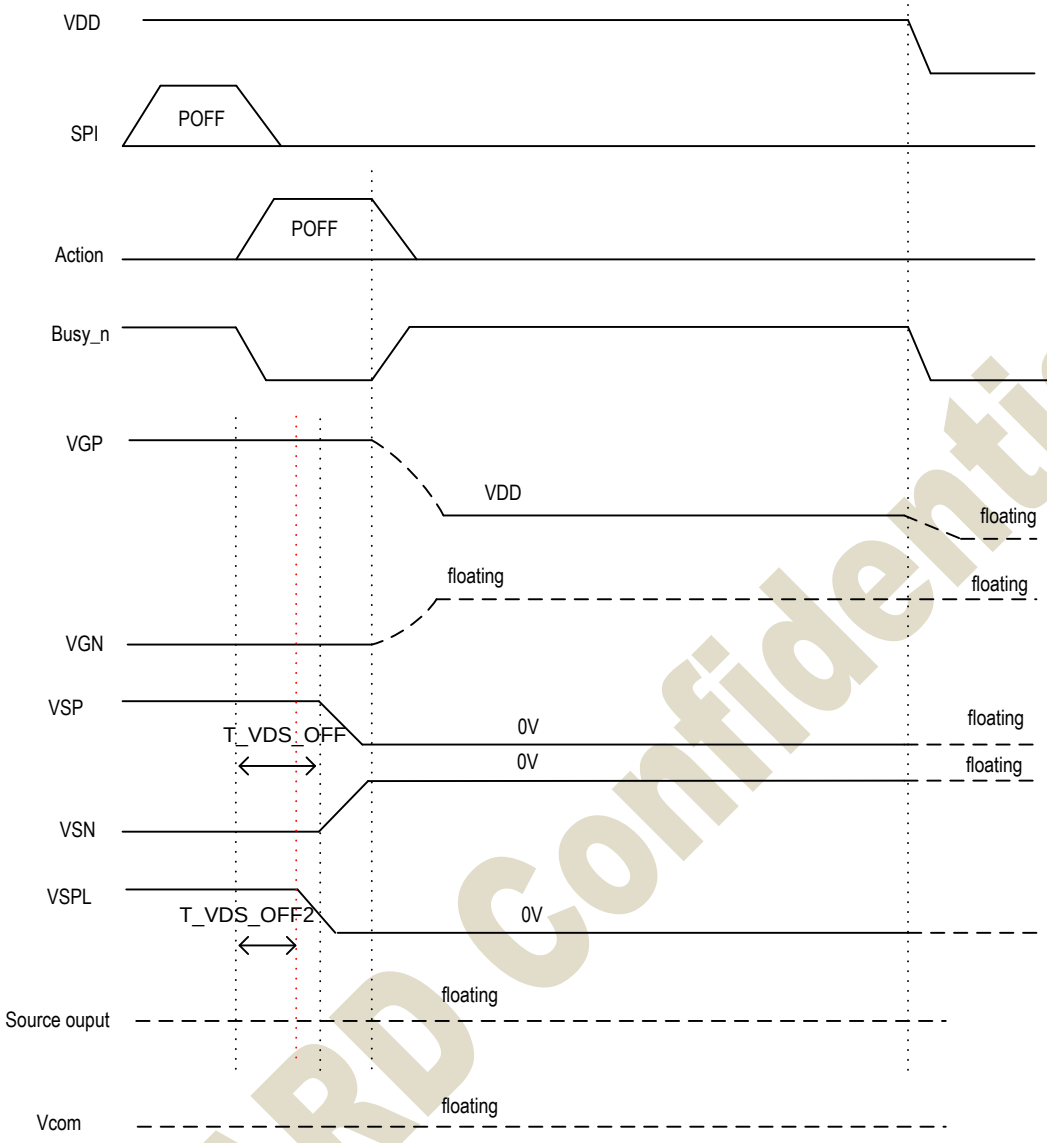


Figure 2: Power off sequence

DSLP sequence

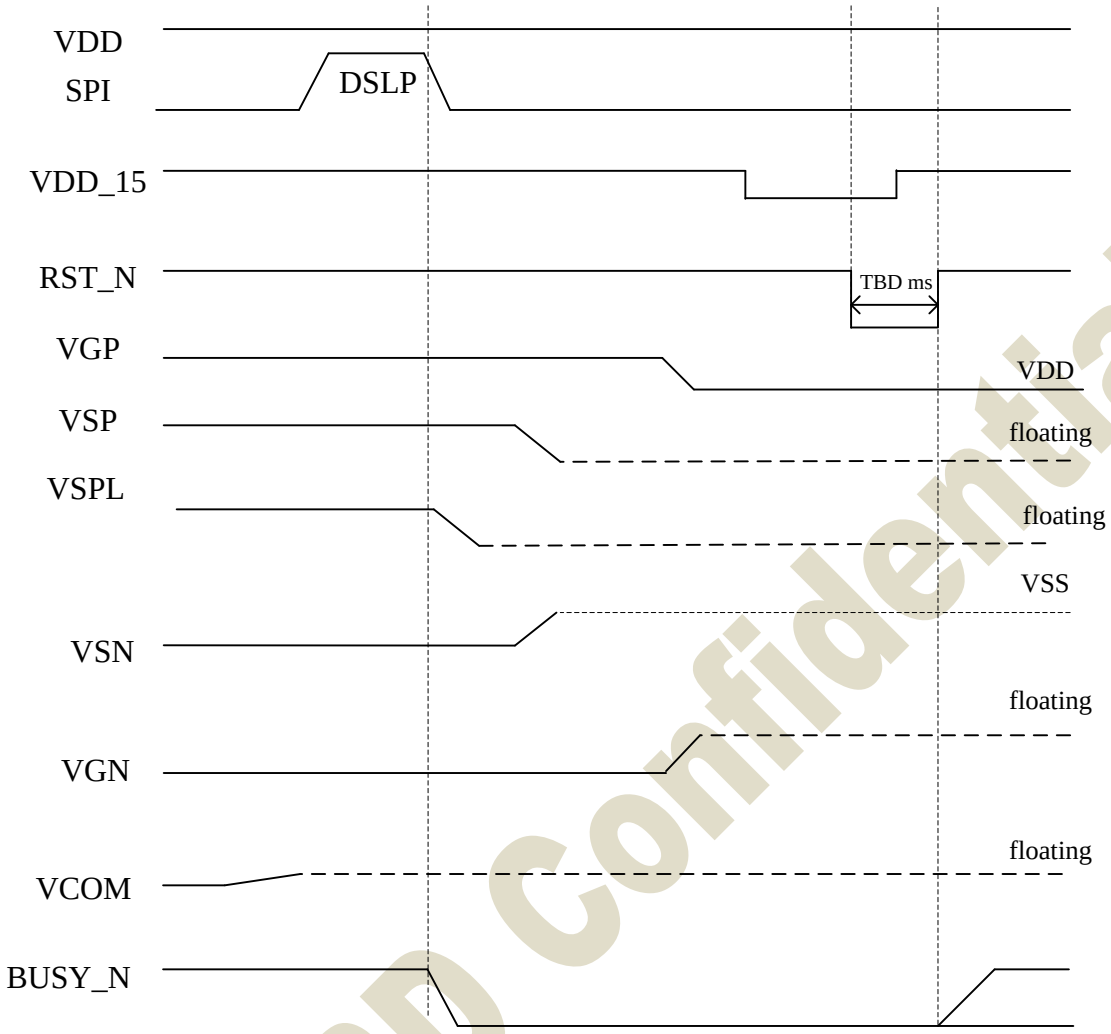


Figure 3: DSLP sequence

9.2 MTP LUT Definition

The MTP size would be 6144 Bytes.

MTP bank 0 (6K bytes)	
Address(Hex)	Content
0x0000~0x15DF	LUT Compress data
0x15E0~0x16F6	Reserved bytes
0x16F7~0X175A	User Reserved bytes(R9FH)
0x175B~0x1784	Default setting
0x1785~0x17FF	JD setting

Default Setting Format in MTP

	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
R9FH	5879-5978	16F7-175A	User Reserved bytes								FF
--	5979	175B	Enable MTP Setting (0xA5)								A5
R00H	5980	175C	RES[1:0]		PST_MODE	-	UD	SHL	SHD_N	RST_N	0F
	5981	176D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09
R01H	5982	175E	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07
	5983	175F	-	-	-		-	-	VGP[1:0]		00
	5984	1760	-	VSPL_0[6:0]							00
	5985	1761	-	VSP_1[6:0]							00
	5986	1762	-	VSN_1[6:0]							00
	5987	1763	-	VSPL_1[6:0]							00
-	5988	1764	Reserved								00
	5989	1765	Reserved								00
	5990	1766	Reserved								54
	5991	1767	Reserved								44
R06H	5992	1768	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00
	5993	1769	-	-	PHA_ON[5:0]						06
	5994	176A	-	-	PHA_OFF[5:0]						02
	5995	176B	-	-	PHB_ON[5:0]						07
	5996	176C	-	-	PHB_OFF[5:0]						02
	5997	176D	-	-	PHC_ON[5:0]						07
	5998	176E	-	-	PHC_OFF[5:0]						02
-	5999	177F	Reserved								00
R30H	6000	1770	-	-	-	-	Dyna	FR[2:0]			02
R50h	6001	1771	VBD[2:0]			DDX	CDI[3:0]				97
-	6002	1772	Reserved								02
	6003	1773	Reserved								02
R61H	6004	1774	-	-	-	-	-	-	HRES[9]	HRES[8]	00
	6005	1775	HRES[7:3]						0	0	00
	6006	1776	-	-	-	-	-	-	VRES[9]	VRES[8]	00
	6007	1777	VRES[7:0]								00
R65H	6008	1778	-	-	-	-	-	-	S_start(9)	S_start(8)	00
	6009	1779	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00
	6010	177A	-	-	-	-	-	-	G_start(9)	G_start(8)	00
	6011	177B	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00
-	6012	177C	Reserved								FF
	6013	177D	Reserved								FF
	6014	177E	Reserved								FF
	6015	177F	Reserved								00
RE3H	6016	1780	VCOM_W[3:0]				SD_W[3:0]				00
RE4H	6017	1781	-	-	-	-	-	-	LVD_SEL[1:0]		03
-	6018	1782	Reserved								03
	6019	1783	Reserved								1C
	6020	1784	Reserved								00
--	6021-6143	1785-17FF	JD setting								FF

9.3 Data transmission waveform

Example1: The driver will scan 1 frame to GND after waveform finished.(FOPT=0)

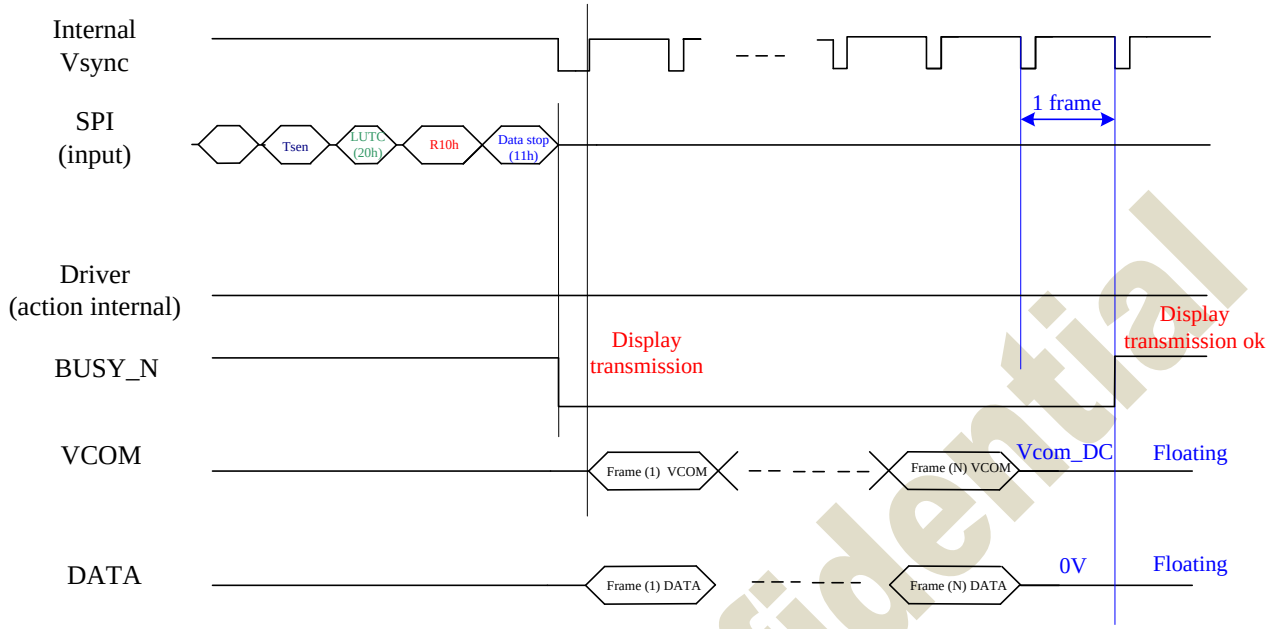


Figure 1: Data transmission example1 waveform

Example2: The driver will float VCOM and keep previous output data(FOPT=1)

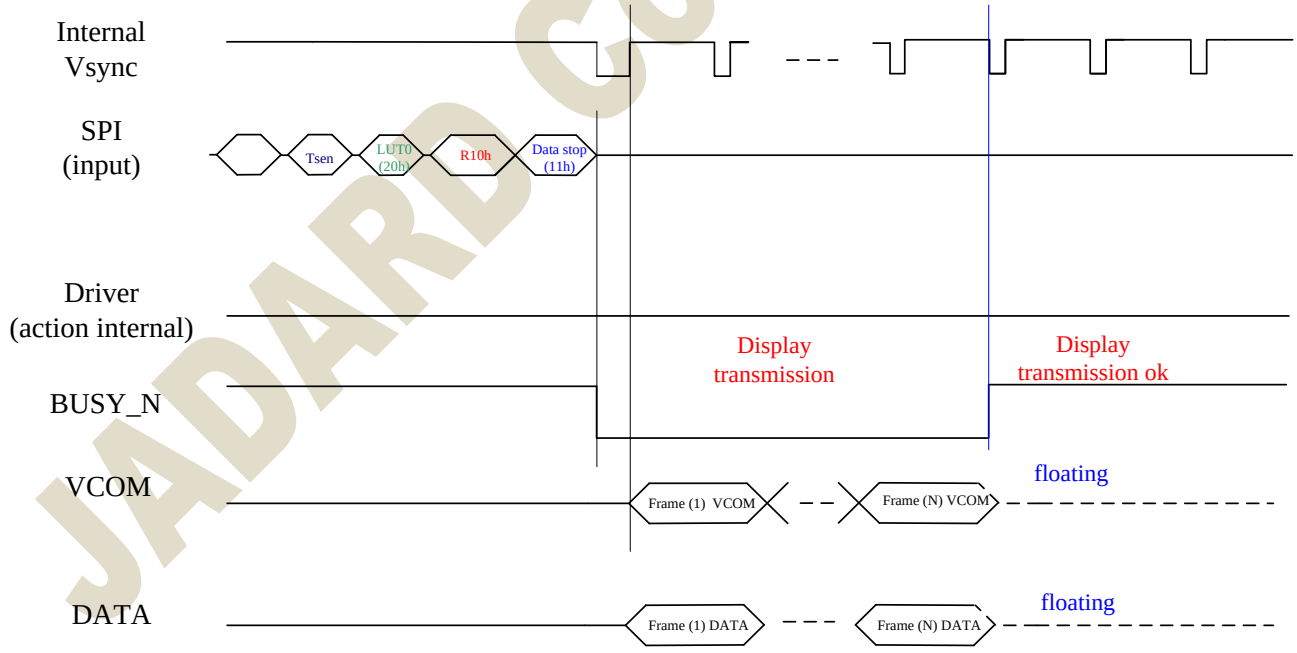


Figure 2: Display refresh example2 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGP-VGN	VGN-0.3	VGP+0.3	V
Analog supply	VSP_0	+15	+15	V
Analog supply	VSN_0	-15	-15	V
Analog supply	VSPL_0	+3	+15	V
Analog supply	VSP_1	+3	+15	V
Analog supply	VSN_1	-3	-15	V
Analog supply	VSPL_1	+3	+15	V
Supply voltage	VGP	+10	+20	V
Supply voltage	VGN	-20	-10	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.5V output voltage	VDD_15	1.35	1.5	1.65		
1.5V input voltage	VDD_15	1.35	1.5	1.65		
MTP program power	VMTP	9.8	10.1	10.2		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3Xvdd	V	Digital input pins
High Level Input Voltage	Vih	0.7Xvio	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400uA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400uA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL= -400 uA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	mA	No load
Operating Current	IVDD1*	-	-	TBD	mA	
Operating temperature	T_{op}	-30	-	85	℃	

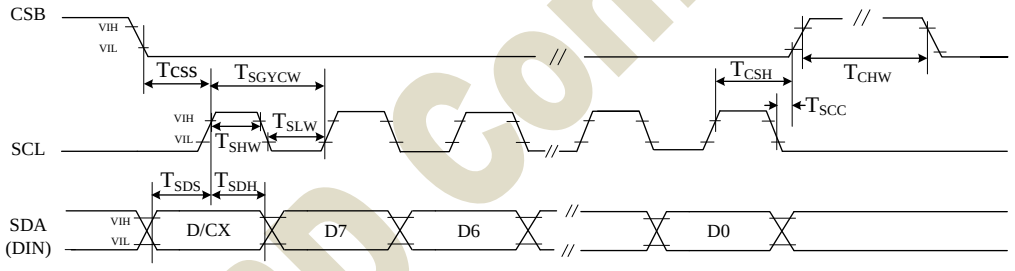
NOTE: typ. and max. values to be confirmed by design

10.3 Analog DC Characteristics

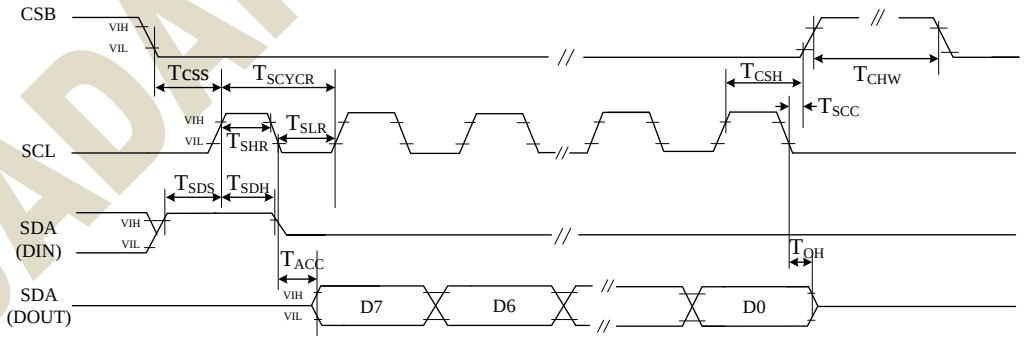
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSP	-	15	-	V	For source driver/VCOM
Positive Source voltage dev	dvsp	-100	0	+100	mV	
Negative Source voltage	VSn	-	-15	-	V	For source driver/VCOM
Negative Source voltage dev	dvsn	-100	-	+100	mV	
Positive Source voltage	VSPL_0	3		15	V	
Positive Source voltage dev.	dvspl_0	-100	-	+100	mV	
Positive Source voltage	VSP_1	3		15	V	
Positive Source voltage dev.	dvsp_1	-100	-	+100	mV	
Positive Source voltage	VSPL_1	3		15	V	
Positive Source voltage dev.	dvspl_1	-100	-	+100	mV	
VCOM voltage dev.	dvcom	-200	-	+200	mV	
Positive gate voltage dev	dvgp	-500	-	+500	mV	
Dynamic Range of Output	Vdr	0.1	-	VSP-0.1	V	
Voltage Range of VGP – VGN	VGP-VGN	-	-	41	V	
Negative Gate voltage	VGN	-10	-	-20	V	For gate driver
Positive Gate voltage	VGP	10		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGP*	-	0	0.2	uA	Include VSP power With load
Positive HV Operating Current	IVGP*	-	0.7	1.1	mA	Include VSP power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGP*	-	0.8	1.2	mA	Include VSP power With load all SD=H VCOM external resistor divider not Included
Negative HV Stand-by Current (power off mode)	IstVGN*	-	0	0.2	uA	Include VSP power With load
Negative HV Operating Current	IVGN*	-	0.8	1.2	mA	Include VSN power With load all SD=L
Negative HV Operating Current	IVGN*	-	0.9-	1.3	mA	Include VSN power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*	-	0	0.01	uA	
VINT1 Operating Current	IVINT1*	-	-	0.3	mA	
Voltage	IVINT1*	-	-	0.3	mA	

10.4 AC Characteristics

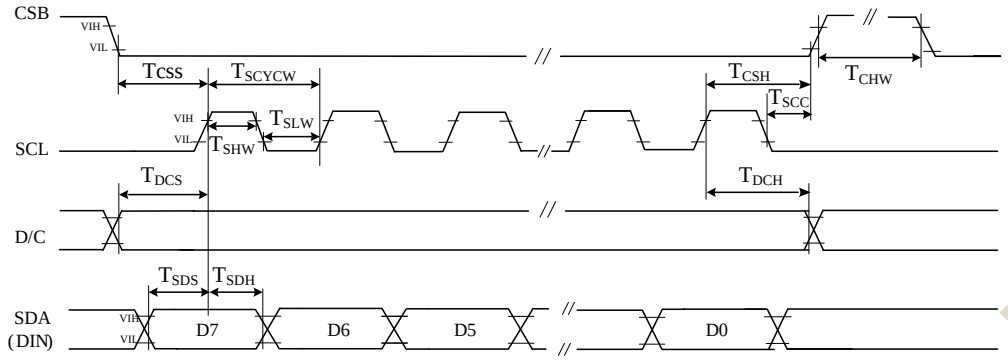
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	150			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time



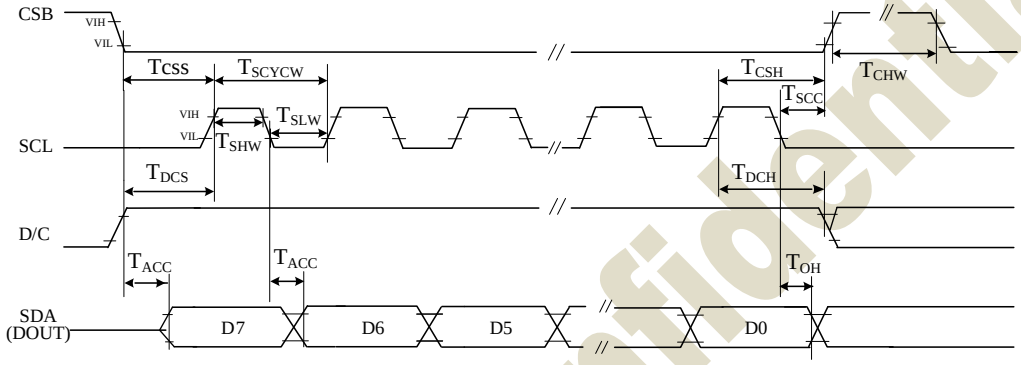
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

Figure 9: SPI interface timing

11. CHIP OUTLINE DIMENSIONS

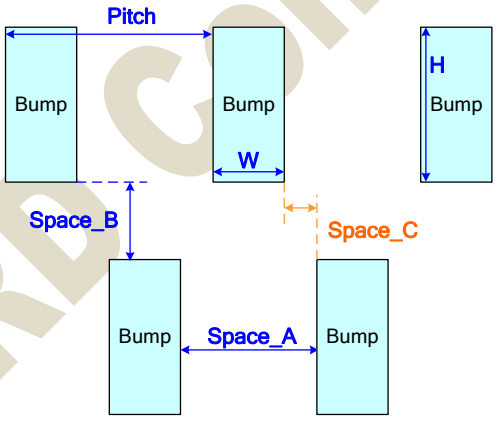
11.1 Circuit/Bump View

G1 G3 G5 ... S_ADDE7~S_ADDE0 S183~S0 S_ADDS7~S_ADDS0 ... G4 G2 G0

JD79667
(face up)

Die Size:	**9900um * 968um**
Die Thickness:	230 μm
Die TTV:	$(D_{MAX} – D_{MIN})$ within die ≤ 2μm
Bump Height:	9 μm ± 2μm
	$(H_{MAX} – H_{MIN})$ within die ≤ 2μm
Hardness:	75 Hv ±25Hv
Coordinate origin:	Chip center

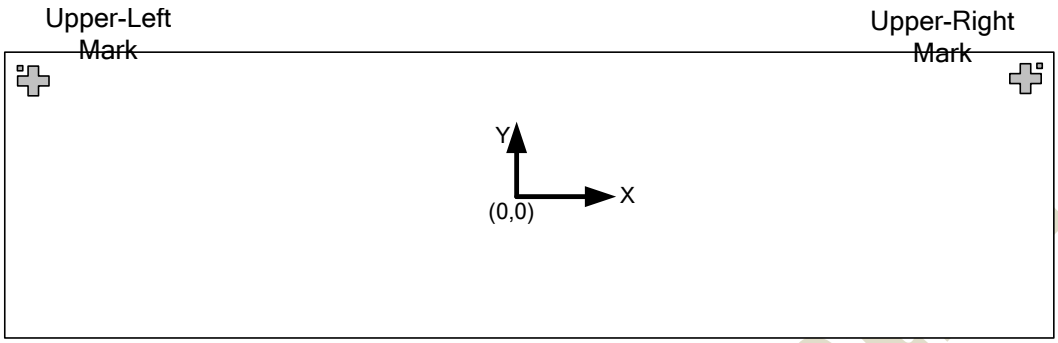
11.2 Bump information



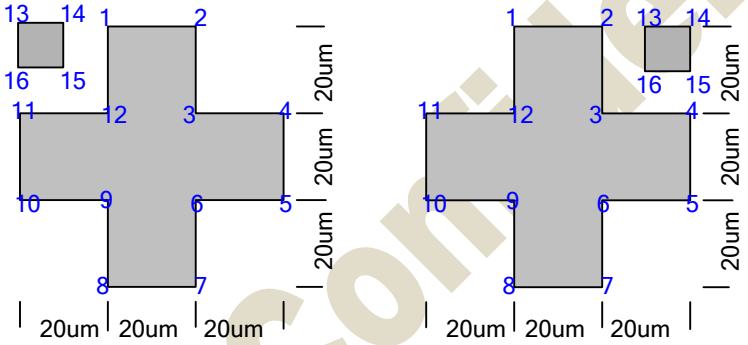
Bump type	Pitch	Space_A	Space_B	Space_C	W	H	Area(um2)	Q'ty	Total Area(um2)
Input PAD	46	18	-	-	28	77.75	2177	211	459347
Source PAD	26	14	19	1	12	90.5	1086	206	223716
Gate PAD	27	15	19	1.5	12	90.5	1086	449	487614
							Total	866	1170677

12. ALIGNMENT MARK INFORMATION

12.1 Location



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-4664.0	382.0	4664.0	382.0
1	-4674.0	412.0	4654.0	412.0
2	-4654.0	412.0	4674.0	412.0
3	-4654.0	392.0	4674.0	392.0
4	-4634.0	392.0	4694.0	392.0
5	-4634.0	372.0	4694.0	372.0
6	-4654.0	372.0	4674.0	372.0
7	-4654.0	352.0	4674.0	352.0
8	-4674.0	352.0	4654.0	352.0
9	-4674.0	372.0	4654.0	372.0
10	-4694.0	372.0	4634.0	372.0
11	-4694.0	392.0	4634.0	392.0
12	-4674.0	392.0	4654.0	392.0
13	-4694.0	412.0	4684.0	412.0
14	-4684.0	412.0	4694.0	412.0
15	-4684.0	402.0	4694.0	402.0
16	-4694.0	402.0	4684.0	402.0

12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	DUMMY[71]	-4830	-404.125	28	77.75
2	DUMMY[72]	-4784	-404.125	28	77.75
3	DUMMY[73]	-4738	-404.125	28	77.75
4	DUMMY[0]	-4692	-404.125	28	77.75
5	DUMMY[1]	-4646	-404.125	28	77.75
6	VCOM	-4600	-404.125	28	77.75
7	VCOM	-4554	-404.125	28	77.75
8	VCOM	-4508	-404.125	28	77.75
9	VCOM	-4462	-404.125	28	77.75
10	VCOM	-4416	-404.125	28	77.75
11	VCOM	-4370	-404.125	28	77.75
12	VCOM	-4324	-404.125	28	77.75
13	VCOM	-4278	-404.125	28	77.75
14	VSSA	-4232	-404.125	28	77.75
15	VGN	-4186	-404.125	28	77.75
16	VGN	-4140	-404.125	28	77.75
17	VGN	-4094	-404.125	28	77.75
18	VGN	-4048	-404.125	28	77.75
19	VGN	-4002	-404.125	28	77.75
20	VGN	-3956	-404.125	28	77.75
21	VGN	-3910	-404.125	28	77.75
22	VGN	-3864	-404.125	28	77.75
23	VGN	-3818	-404.125	28	77.75
24	VGN	-3772	-404.125	28	77.75
25	VGN	-3726	-404.125	28	77.75
26	VGN	-3680	-404.125	28	77.75
27	VGN	-3634	-404.125	28	77.75
28	VGN	-3588	-404.125	28	77.75
29	VGN	-3542	-404.125	28	77.75
30	VGN	-3496	-404.125	28	77.75
31	VSSA	-3450	-404.125	28	77.75
32	VSN	-3404	-404.125	28	77.75
33	VSN	-3358	-404.125	28	77.75
34	VSN	-3312	-404.125	28	77.75
35	VSN	-3266	-404.125	28	77.75
36	VSN	-3220	-404.125	28	77.75
37	VSN	-3174	-404.125	28	77.75
38	VSN	-3128	-404.125	28	77.75
39	VSN	-3082	-404.125	28	77.75
40	VSN	-3036	-404.125	28	77.75
41	VSN	-2990	-404.125	28	77.75
42	VSSA	-2944	-404.125	28	77.75
43	VGP	-2898	-404.125	28	77.75
44	VGP	-2852	-404.125	28	77.75
45	VGP	-2806	-404.125	28	77.75
46	VGP	-2760	-404.125	28	77.75
47	VGP	-2714	-404.125	28	77.75
48	VGP	-2668	-404.125	28	77.75
49	VGP	-2622	-404.125	28	77.75
50	VGP	-2576	-404.125	28	77.75
51	VGP	-2530	-404.125	28	77.75
52	VGP	-2484	-404.125	28	77.75
53	VGP	-2438	-404.125	28	77.75
54	VGP	-2392	-404.125	28	77.75
55	VSSA	-2346	-404.125	28	77.75
56	VSP	-2300	-404.125	28	77.75
57	VSP	-2254	-404.125	28	77.75
58	VSP	-2208	-404.125	28	77.75

No.	Name	X-axis	Y-axis	W	H
59	VSP	-2162	-404.125	28	77.75
60	VSP	-2116	-404.125	28	77.75
61	VSP	-2070	-404.125	28	77.75
62	VSP	-2024	-404.125	28	77.75
63	VSP	-1978	-404.125	28	77.75
64	VSP	-1932	-404.125	28	77.75
65	VSP	-1886	-404.125	28	77.75
66	VSSA	-1840	-404.125	28	77.75
67	VMTP	-1794	-404.125	28	77.75
68	VMTP	-1748	-404.125	28	77.75
69	VMTP	-1702	-404.125	28	77.75
70	VMTP	-1656	-404.125	28	77.75
71	VMTP	-1610	-404.125	28	77.75
72	VMTP	-1564	-404.125	28	77.75
73	VDD_15V	-1518	-404.125	28	77.75
74	VDD_15V	-1472	-404.125	28	77.75
75	VDD_15V	-1426	-404.125	28	77.75
76	VDD_15V	-1380	-404.125	28	77.75
77	VDD_15V	-1334	-404.125	28	77.75
78	VDD_15V	-1288	-404.125	28	77.75
79	VDD_15V	-1242	-404.125	28	77.75
80	VDD_15V	-1196	-404.125	28	77.75
81	VSSA	-1150	-404.125	28	77.75
82	VSSA	-1104	-404.125	28	77.75
83	VSSA	-1058	-404.125	28	77.75
84	VSSA	-1012	-404.125	28	77.75
85	VSSA	-966	-404.125	28	77.75
86	VSSA	-920	-404.125	28	77.75
87	VSSA	-874	-404.125	28	77.75
88	VSSA	-828	-404.125	28	77.75
89	VSSA	-782	-404.125	28	77.75
90	VSSA	-736	-404.125	28	77.75
91	VSSA	-690	-404.125	28	77.75
92	VSSA	-644	-404.125	28	77.75
93	VSS	-598	-404.125	28	77.75
94	VSS	-552	-404.125	28	77.75
95	VSS	-506	-404.125	28	77.75
96	VSS	-460	-404.125	28	77.75
97	VSS	-414	-404.125	28	77.75
98	VSS	-368	-404.125	28	77.75
99	VSS	-322	-404.125	28	77.75
100	VSS	-276	-404.125	28	77.75
101	VSS	-230	-404.125	28	77.75
102	VSS	-184	-404.125	28	77.75
103	T_IN[1]	-138	-404.125	28	77.75
104	T_IN[0]	-92	-404.125	28	77.75
105	VDD	-46	-404.125	28	77.75
106	VDD	0	-404.125	28	77.75
107	VDD	46	-404.125	28	77.75
108	VDD	92	-404.125	28	77.75
109	VDD	138	-404.125	28	77.75
110	VDD	184	-404.125	28	77.75
111	VDD	230	-404.125	28	77.75
112	VDD	276	-404.125	28	77.75
113	VDD	322	-404.125	28	77.75
114	VDD	368	-404.125	28	77.75
115	VDDIO	414	-404.125	28	77.75
116	VDDIO	460	-404.125	28	77.75

No.	Name	X-axis	Y-axis	W	H
117	VDDIO	506	-404.125	28	77.75
118	VDDIO	552	-404.125	28	77.75
119	VDDIO	598	-404.125	28	77.75
120	VDDIO	644	-404.125	28	77.75
121	VDDIO	690	-404.125	28	77.75
122	T_DEBUG[7]	736	-404.125	28	77.75
123	T_DEBUG[6]	782	-404.125	28	77.75
124	VDDP	828	-404.125	28	77.75
125	VDDP	874	-404.125	28	77.75
126	VDDP	920	-404.125	28	77.75
127	VDDP	966	-404.125	28	77.75
128	T_DEBUG[5]	1012	-404.125	28	77.75
129	T_DEBUG[4]	1058	-404.125	28	77.75
130	T_DEBUG[4]	1104	-404.125	28	77.75
131	T_DEBUG[3]	1150	-404.125	28	77.75
132	T_DEBUG[3]	1196	-404.125	28	77.75
133	DUMMY[2]	1242	-404.125	28	77.75
134	SDA	1288	-404.125	28	77.75
135	SCL	1334	-404.125	28	77.75
136	DUMMY[91]	1380	-404.125	28	77.75
137	CSB	1426	-404.125	28	77.75
138	DUMMY[92]	1472	-404.125	28	77.75
139	T_DEBUG[2]	1518	-404.125	28	77.75
140	DUMMY[93]	1564	-404.125	28	77.75
141	DC	1610	-404.125	28	77.75
142	DUMMY[94]	1656	-404.125	28	77.75
143	T_DEBUG[1]	1702	-404.125	28	77.75
144	DUMMY[95]	1748	-404.125	28	77.75
145	RST_N	1794	-404.125	28	77.75
146	BUSY_N	1840	-404.125	28	77.75
147	SYNCC	1886	-404.125	28	77.75
148	DUMMY[96]	1932	-404.125	28	77.75
149	T_DEBUG[8]	1978	-404.125	28	77.75
150	VSS	2024	-404.125	28	77.75
151	T_DEBUG[0]	2070	-404.125	28	77.75
152	VDDIO	2116	-404.125	28	77.75
153	BS	2162	-404.125	28	77.75
154	VSS	2208	-404.125	28	77.75
155	T_EN_DIG	2254	-404.125	28	77.75
156	VDDIO	2300	-404.125	28	77.75
157	PCKI	2346	-404.125	28	77.75
158	VSS	2392	-404.125	28	77.75
159	MS	2438	-404.125	28	77.75
160	VDDIO	2484	-404.125	28	77.75
161	TSDA	2530	-404.125	28	77.75
162	TSDA	2576	-404.125	28	77.75
163	TSCL	2622	-404.125	28	77.75
164	TSCL	2668	-404.125	28	77.75
165	PCKO	2714	-404.125	28	77.75
166	SYNCD	2760	-404.125	28	77.75
167	T_EX_SYSCLK	2806	-404.125	28	77.75
168	T_EX_REFCLK	2852	-404.125	28	77.75
169	VSPL	2898	-404.125	28	77.75
170	VSPL	2944	-404.125	28	77.75
171	VSPL	2990	-404.125	28	77.75
172	VSPL	3036	-404.125	28	77.75
173	VSPL	3082	-404.125	28	77.75
174	VSPL	3128	-404.125	28	77.75
175	VSPL	3174	-404.125	28	77.75
176	VSPL	3220	-404.125	28	77.75

No.	Name	X-axis	Y-axis	W	H
177	DUMMY[3]	3266	-404.125	28	77.75
178	DUMMY[4]	3312	-404.125	28	77.75
179	DUMMY[5]	3358	-404.125	28	77.75
180	DUMMY[6]	3404	-404.125	28	77.75
181	DUMMY[7]	3450	-404.125	28	77.75
182	DUMMY[8]	3496	-404.125	28	77.75
183	VSSA	3542	-404.125	28	77.75
184	FB	3588	-404.125	28	77.75
185	FB	3634	-404.125	28	77.75
186	DUMMY[97]	3680	-404.125	28	77.75
187	RESE	3726	-404.125	28	77.75
188	RESE	3772	-404.125	28	77.75
189	VSSA	3818	-404.125	28	77.75
190	GDR	3864	-404.125	28	77.75
191	GDR	3910	-404.125	28	77.75
192	GDR	3956	-404.125	28	77.75
193	GDR	4002	-404.125	28	77.75
194	GDR	4048	-404.125	28	77.75
195	GDR	4094	-404.125	28	77.75
196	GDR	4140	-404.125	28	77.75
197	GDR	4186	-404.125	28	77.75
198	VSSA	4232	-404.125	28	77.75
199	VCOM	4278	-404.125	28	77.75
200	VCOM	4324	-404.125	28	77.75
201	VCOM	4370	-404.125	28	77.75
202	VCOM	4416	-404.125	28	77.75
203	VCOM	4462	-404.125	28	77.75
204	VCOM	4508	-404.125	28	77.75
205	VCOM	4554	-404.125	28	77.75
206	VCOM	4600	-404.125	28	77.75
207	DUMMY[9]	4646	-404.125	28	77.75
208	DUMMY[10]	4692	-404.125	28	77.75
209	DUMMY[74]	4738	-404.125	28	77.75
210	DUMMY[75]	4784	-404.125	28	77.75
211	DUMMY[76]	4830	-404.125	28	77.75
212	DUMMY[79]	4730	286.75	12	90.5
213	DUMMY[78]	4770	286.75	12	90.5
214	DUMMY[77]	4810	286.75	12	90.5
215	DUMMY[80]	4588.5	396.25	12	90.5
216	DUMMY[81]	4548.5	396.25	12	90.5
217	DUMMY[82]	4508.5	396.25	12	90.5
218	DUMMY[83]	4468.5	396.25	12	90.5
219	DUMMY[11]	4428.5	396.25	12	90.5
220	DUMMY[12]	4415	286.75	12	90.5
221	DUMMY[13]	4401.5	396.25	12	90.5
222	DUMMY[14]	4388	286.75	12	90.5
223	DUMMY[15]	4374.5	396.25	12	90.5
224	DUMMY[16]	4361	286.75	12	90.5
225	T_VREF	4347.5	396.25	12	90.5
226	T_EN_LSH	4334	286.75	12	90.5
227	T_IBIAS	4320.5	396.25	12	90.5
228	T_VTSEN	4307	286.75	12	90.5
229	DUMMY[17]	4293.5	396.25	12	90.5
230	T_SAR_REF	4280	286.75	12	90.5
231	G[0]	4266.5	396.25	12	90.5
232	G[2]	4253	286.75	12	90.5
233	G[4]	4239.5	396.25	12	90.5
234	G[6]	4226	286.75	12	90.5
235	G[8]	4212.5	396.25	12	90.5
236	G[10]	4199	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
237	G[12]	4185.5	396.25	12	90.5
238	G[14]	4172	286.75	12	90.5
239	G[16]	4158.5	396.25	12	90.5
240	G[18]	4145	286.75	12	90.5
241	G[20]	4131.5	396.25	12	90.5
242	G[22]	4118	286.75	12	90.5
243	G[24]	4104.5	396.25	12	90.5
244	G[26]	4091	286.75	12	90.5
245	G[28]	4077.5	396.25	12	90.5
246	G[30]	4064	286.75	12	90.5
247	G[32]	4050.5	396.25	12	90.5
248	G[34]	4037	286.75	12	90.5
249	G[36]	4023.5	396.25	12	90.5
250	G[38]	4010	286.75	12	90.5
251	G[40]	3996.5	396.25	12	90.5
252	G[42]	3983	286.75	12	90.5
253	G[44]	3969.5	396.25	12	90.5
254	G[46]	3956	286.75	12	90.5
255	G[48]	3942.5	396.25	12	90.5
256	G[50]	3929	286.75	12	90.5
257	G[52]	3915.5	396.25	12	90.5
258	G[54]	3902	286.75	12	90.5
259	G[56]	3888.5	396.25	12	90.5
260	G[58]	3875	286.75	12	90.5
261	G[60]	3861.5	396.25	12	90.5
262	G[62]	3848	286.75	12	90.5
263	G[64]	3834.5	396.25	12	90.5
264	G[66]	3821	286.75	12	90.5
265	G[68]	3807.5	396.25	12	90.5
266	G[70]	3794	286.75	12	90.5
267	G[72]	3780.5	396.25	12	90.5
268	G[74]	3767	286.75	12	90.5
269	G[76]	3753.5	396.25	12	90.5
270	G[78]	3740	286.75	12	90.5
271	G[80]	3726.5	396.25	12	90.5
272	G[82]	3713	286.75	12	90.5
273	G[84]	3699.5	396.25	12	90.5
274	G[86]	3686	286.75	12	90.5
275	G[88]	3672.5	396.25	12	90.5
276	G[90]	3659	286.75	12	90.5
277	G[92]	3645.5	396.25	12	90.5
278	G[94]	3632	286.75	12	90.5
279	G[96]	3618.5	396.25	12	90.5
280	G[98]	3605	286.75	12	90.5
281	G[100]	3591.5	396.25	12	90.5
282	G[102]	3578	286.75	12	90.5
283	G[104]	3564.5	396.25	12	90.5
284	G[106]	3551	286.75	12	90.5
285	G[108]	3537.5	396.25	12	90.5
286	G[110]	3524	286.75	12	90.5
287	G[112]	3510.5	396.25	12	90.5
288	G[114]	3497	286.75	12	90.5
289	G[116]	3483.5	396.25	12	90.5
290	G[118]	3470	286.75	12	90.5
291	G[120]	3456.5	396.25	12	90.5
292	G[122]	3443	286.75	12	90.5
293	G[124]	3429.5	396.25	12	90.5
294	G[126]	3416	286.75	12	90.5
295	G[128]	3402.5	396.25	12	90.5
296	G[130]	3389	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
297	G[132]	3375.5	396.25	12	90.5
298	G[134]	3362	286.75	12	90.5
299	G[136]	3348.5	396.25	12	90.5
300	G[138]	3335	286.75	12	90.5
301	G[140]	3321.5	396.25	12	90.5
302	G[142]	3308	286.75	12	90.5
303	G[144]	3294.5	396.25	12	90.5
304	G[146]	3281	286.75	12	90.5
305	G[148]	3267.5	396.25	12	90.5
306	G[150]	3254	286.75	12	90.5
307	G[152]	3240.5	396.25	12	90.5
308	G[154]	3227	286.75	12	90.5
309	G[156]	3213.5	396.25	12	90.5
310	G[158]	3200	286.75	12	90.5
311	G[160]	3186.5	396.25	12	90.5
312	G[162]	3173	286.75	12	90.5
313	G[164]	3159.5	396.25	12	90.5
314	G[166]	3146	286.75	12	90.5
315	G[168]	3132.5	396.25	12	90.5
316	G[170]	3119	286.75	12	90.5
317	G[172]	3105.5	396.25	12	90.5
318	G[174]	3092	286.75	12	90.5
319	G[176]	3078.5	396.25	12	90.5
320	G[178]	3065	286.75	12	90.5
321	G[180]	3051.5	396.25	12	90.5
322	G[182]	3038	286.75	12	90.5
323	G[184]	3024.5	396.25	12	90.5
324	G[186]	3011	286.75	12	90.5
325	G[188]	2997.5	396.25	12	90.5
326	G[190]	2984	286.75	12	90.5
327	G[192]	2970.5	396.25	12	90.5
328	G[194]	2957	286.75	12	90.5
329	G[196]	2943.5	396.25	12	90.5
330	G[198]	2930	286.75	12	90.5
331	G[200]	2916.5	396.25	12	90.5
332	G[202]	2903	286.75	12	90.5
333	G[204]	2889.5	396.25	12	90.5
334	G[206]	2876	286.75	12	90.5
335	G[208]	2862.5	396.25	12	90.5
336	G[210]	2849	286.75	12	90.5
337	G[212]	2835.5	396.25	12	90.5
338	G[214]	2822	286.75	12	90.5
339	G[216]	2808.5	396.25	12	90.5
340	G[218]	2795	286.75	12	90.5
341	G[220]	2781.5	396.25	12	90.5
342	G[222]	2768	286.75	12	90.5
343	G[224]	2754.5	396.25	12	90.5
344	G[226]	2741	286.75	12	90.5
345	G[228]	2727.5	396.25	12	90.5
346	G[230]	2714	286.75	12	90.5
347	G[232]	2700.5	396.25	12	90.5
348	G[234]	2687	286.75	12	90.5
349	G[236]	2673.5	396.25	12	90.5
350	G[238]	2660	286.75	12	90.5
351	G[240]	2646.5	396.25	12	90.5
352	G[242]	2633	286.75	12	90.5
353	G[244]	2619.5	396.25	12	90.5
354	G[246]	2606	286.75	12	90.5
355	G[248]	2592.5	396.25	12	90.5
356	G[250]	2579	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
357	G[252]	2565.5	396.25	12	90.5
358	G[254]	2552	286.75	12	90.5
359	G[256]	2538.5	396.25	12	90.5
360	G[258]	2525	286.75	12	90.5
361	G[260]	2511.5	396.25	12	90.5
362	G[262]	2498	286.75	12	90.5
363	G[264]	2484.5	396.25	12	90.5
364	G[266]	2471	286.75	12	90.5
365	G[268]	2457.5	396.25	12	90.5
366	G[270]	2444	286.75	12	90.5
367	G[272]	2430.5	396.25	12	90.5
368	G[274]	2417	286.75	12	90.5
369	G[276]	2403.5	396.25	12	90.5
370	G[278]	2390	286.75	12	90.5
371	G[280]	2376.5	396.25	12	90.5
372	G[282]	2363	286.75	12	90.5
373	G[284]	2349.5	396.25	12	90.5
374	G[286]	2336	286.75	12	90.5
375	G[288]	2322.5	396.25	12	90.5
376	G[290]	2309	286.75	12	90.5
377	G[292]	2295.5	396.25	12	90.5
378	G[294]	2282	286.75	12	90.5
379	G[296]	2268.5	396.25	12	90.5
380	G[298]	2255	286.75	12	90.5
381	G[300]	2241.5	396.25	12	90.5
382	G[302]	2228	286.75	12	90.5
383	G[304]	2214.5	396.25	12	90.5
384	G[306]	2201	286.75	12	90.5
385	G[308]	2187.5	396.25	12	90.5
386	G[310]	2174	286.75	12	90.5
387	G[312]	2160.5	396.25	12	90.5
388	G[314]	2147	286.75	12	90.5
389	G[316]	2133.5	396.25	12	90.5
390	G[318]	2120	286.75	12	90.5
391	G[320]	2106.5	396.25	12	90.5
392	G[322]	2093	286.75	12	90.5
393	G[324]	2079.5	396.25	12	90.5
394	G[326]	2066	286.75	12	90.5
395	G[328]	2052.5	396.25	12	90.5
396	G[330]	2039	286.75	12	90.5
397	G[332]	2025.5	396.25	12	90.5
398	G[334]	2012	286.75	12	90.5
399	G[336]	1998.5	396.25	12	90.5
400	G[338]	1985	286.75	12	90.5
401	G[340]	1971.5	396.25	12	90.5
402	G[342]	1958	286.75	12	90.5
403	G[344]	1944.5	396.25	12	90.5
404	G[346]	1931	286.75	12	90.5
405	G[348]	1917.5	396.25	12	90.5
406	G[350]	1904	286.75	12	90.5
407	G[352]	1890.5	396.25	12	90.5
408	G[354]	1877	286.75	12	90.5
409	G[356]	1863.5	396.25	12	90.5
410	G[358]	1850	286.75	12	90.5
411	G[360]	1836.5	396.25	12	90.5
412	G[362]	1823	286.75	12	90.5
413	G[364]	1809.5	396.25	12	90.5
414	G[366]	1796	286.75	12	90.5
415	G[368]	1782.5	396.25	12	90.5
416	G[370]	1769	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
417	G[372]	1755.5	396.25	12	90.5
418	G[374]	1742	286.75	12	90.5
419	G[376]	1728.5	396.25	12	90.5
420	G[378]	1715	286.75	12	90.5
421	G[380]	1701.5	396.25	12	90.5
422	G[382]	1688	286.75	12	90.5
423	DUMMY[18]	1674.5	396.25	12	90.5
424	DUMMY[19]	1661	286.75	12	90.5
425	DUMMY[20]	1647.5	396.25	12	90.5
426	DUMMY[21]	1634	286.75	12	90.5
427	DUMMY[22]	1620.5	396.25	12	90.5
428	DUMMY[23]	1607	286.75	12	90.5
429	DUMMY[24]	1593.5	396.25	12	90.5
430	DUMMY[25]	1580	286.75	12	90.5
431	DUMMY[26]	1566.5	396.25	12	90.5
432	DUMMY[27]	1553	286.75	12	90.5
433	DUMMY[28]	1539.5	396.25	12	90.5
434	DUMMY[29]	1526	286.75	12	90.5
435	DUMMY[30]	1512.5	396.25	12	90.5
436	DUMMY[31]	1499	286.75	12	90.5
437	DUMMY[32]	1332.5	397.75	12	90.5
438	DUMMY[33]	1319.5	288.25	12	90.5
439	VBD1	1306.5	397.75	12	90.5
440	DUMMY[34]	1293.5	288.25	12	90.5
441	DUMMY[35]	1280.5	397.75	12	90.5
442	DUMMY[36]	1267.5	288.25	12	90.5
443	DUMMY[37]	1254.5	397.75	12	90.5
444	DUMMY[38]	1241.5	288.25	12	90.5
445	DUMMY[39]	1228.5	397.75	12	90.5
446	DUMMY[40]	1215.5	288.25	12	90.5
447	DUMMY[41]	1202.5	397.75	12	90.5
448	S[0]	1189.5	288.25	12	90.5
449	S[1]	1176.5	397.75	12	90.5
450	S[2]	1163.5	288.25	12	90.5
451	S[3]	1150.5	397.75	12	90.5
452	S[4]	1137.5	288.25	12	90.5
453	S[5]	1124.5	397.75	12	90.5
454	S[6]	1111.5	288.25	12	90.5
455	S[7]	1098.5	397.75	12	90.5
456	S[8]	1085.5	288.25	12	90.5
457	S[9]	1072.5	397.75	12	90.5
458	S[10]	1059.5	288.25	12	90.5
459	S[11]	1046.5	397.75	12	90.5
460	S[12]	1033.5	288.25	12	90.5
461	S[13]	1020.5	397.75	12	90.5
462	S[14]	1007.5	288.25	12	90.5
463	S[15]	994.5	397.75	12	90.5
464	S[16]	981.5	288.25	12	90.5
465	S[17]	968.5	397.75	12	90.5
466	S[18]	955.5	288.25	12	90.5
467	S[19]	942.5	397.75	12	90.5
468	S[20]	929.5	288.25	12	90.5
469	S[21]	916.5	397.75	12	90.5
470	S[22]	903.5	288.25	12	90.5
471	S[23]	890.5	397.75	12	90.5
472	S[24]	877.5	288.25	12	90.5
473	S[25]	864.5	397.75	12	90.5
474	S[26]	851.5	288.25	12	90.5
475	S[27]	838.5	397.75	12	90.5
476	S[28]	825.5	288.25	12	90.5

No.	Name	X-axis	Y-axis	W	H
477	S[29]	812.5	397.75	12	90.5
478	S[30]	799.5	288.25	12	90.5
479	S[31]	786.5	397.75	12	90.5
480	S[32]	773.5	288.25	12	90.5
481	S[33]	760.5	397.75	12	90.5
482	S[34]	747.5	288.25	12	90.5
483	S[35]	734.5	397.75	12	90.5
484	S[36]	721.5	288.25	12	90.5
485	S[37]	708.5	397.75	12	90.5
486	S[38]	695.5	288.25	12	90.5
487	S[39]	682.5	397.75	12	90.5
488	S[40]	669.5	288.25	12	90.5
489	S[41]	656.5	397.75	12	90.5
490	S[42]	643.5	288.25	12	90.5
491	S[43]	630.5	397.75	12	90.5
492	S[44]	617.5	288.25	12	90.5
493	S[45]	604.5	397.75	12	90.5
494	S[46]	591.5	288.25	12	90.5
495	S[47]	578.5	397.75	12	90.5
496	S[48]	565.5	288.25	12	90.5
497	S[49]	552.5	397.75	12	90.5
498	S[50]	539.5	288.25	12	90.5
499	S[51]	526.5	397.75	12	90.5
500	S[52]	513.5	288.25	12	90.5
501	S[53]	500.5	397.75	12	90.5
502	S[54]	487.5	288.25	12	90.5
503	S[55]	474.5	397.75	12	90.5
504	S[56]	461.5	288.25	12	90.5
505	S[57]	448.5	397.75	12	90.5
506	S[58]	435.5	288.25	12	90.5
507	S[59]	422.5	397.75	12	90.5
508	S[60]	409.5	288.25	12	90.5
509	S[61]	396.5	397.75	12	90.5
510	S[62]	383.5	288.25	12	90.5
511	S[63]	370.5	397.75	12	90.5
512	S[64]	357.5	288.25	12	90.5
513	S[65]	344.5	397.75	12	90.5
514	S[66]	331.5	288.25	12	90.5
515	S[67]	318.5	397.75	12	90.5
516	S[68]	305.5	288.25	12	90.5
517	S[69]	292.5	397.75	12	90.5
518	S[70]	279.5	288.25	12	90.5
519	S[71]	266.5	397.75	12	90.5
520	S[72]	253.5	288.25	12	90.5
521	S[73]	240.5	397.75	12	90.5
522	S[74]	227.5	288.25	12	90.5
523	S[75]	214.5	397.75	12	90.5
524	S[76]	201.5	288.25	12	90.5
525	S[77]	188.5	397.75	12	90.5
526	S[78]	175.5	288.25	12	90.5
527	S[79]	162.5	397.75	12	90.5
528	S[80]	149.5	288.25	12	90.5
529	S[81]	136.5	397.75	12	90.5
530	S[82]	123.5	288.25	12	90.5
531	S[83]	110.5	397.75	12	90.5
532	S[84]	97.5	288.25	12	90.5
533	S[85]	84.5	397.75	12	90.5
534	S[86]	71.5	288.25	12	90.5
535	S[87]	58.5	397.75	12	90.5
536	S[88]	45.5	288.25	12	90.5

No.	Name	X-axis	Y-axis	W	H
537	S[89]	32.5	397.75	12	90.5
538	S[90]	19.5	288.25	12	90.5
539	S[91]	6.5	397.75	12	90.5
540	S[92]	-6.5	288.25	12	90.5
541	S[93]	-19.5	397.75	12	90.5
542	S[94]	-32.5	288.25	12	90.5
543	S[95]	-45.5	397.75	12	90.5
544	S[96]	-58.5	288.25	12	90.5
545	S[97]	-71.5	397.75	12	90.5
546	S[98]	-84.5	288.25	12	90.5
547	S[99]	-97.5	397.75	12	90.5
548	S[100]	-110.5	288.25	12	90.5
549	S[101]	-123.5	397.75	12	90.5
550	S[102]	-136.5	288.25	12	90.5
551	S[103]	-149.5	397.75	12	90.5
552	S[104]	-162.5	288.25	12	90.5
553	S[105]	-175.5	397.75	12	90.5
554	S[106]	-188.5	288.25	12	90.5
555	S[107]	-201.5	397.75	12	90.5
556	S[108]	-214.5	288.25	12	90.5
557	S[109]	-227.5	397.75	12	90.5
558	S[110]	-240.5	288.25	12	90.5
559	S[111]	-253.5	397.75	12	90.5
560	S[112]	-266.5	288.25	12	90.5
561	S[113]	-279.5	397.75	12	90.5
562	S[114]	-292.5	288.25	12	90.5
563	S[115]	-305.5	397.75	12	90.5
564	S[116]	-318.5	288.25	12	90.5
565	S[117]	-331.5	397.75	12	90.5
566	S[118]	-344.5	288.25	12	90.5
567	S[119]	-357.5	397.75	12	90.5
568	S[120]	-370.5	288.25	12	90.5
569	S[121]	-383.5	397.75	12	90.5
570	S[122]	-396.5	288.25	12	90.5
571	S[123]	-409.5	397.75	12	90.5
572	S[124]	-422.5	288.25	12	90.5
573	S[125]	-435.5	397.75	12	90.5
574	S[126]	-448.5	288.25	12	90.5
575	S[127]	-461.5	397.75	12	90.5
576	S[128]	-474.5	288.25	12	90.5
577	S[129]	-487.5	397.75	12	90.5
578	S[130]	-500.5	288.25	12	90.5
579	S[131]	-513.5	397.75	12	90.5
580	S[132]	-526.5	288.25	12	90.5
581	S[133]	-539.5	397.75	12	90.5
582	S[134]	-552.5	288.25	12	90.5
583	S[135]	-565.5	397.75	12	90.5
584	S[136]	-578.5	288.25	12	90.5
585	S[137]	-591.5	397.75	12	90.5
586	S[138]	-604.5	288.25	12	90.5
587	S[139]	-617.5	397.75	12	90.5
588	S[140]	-630.5	288.25	12	90.5
589	S[141]	-643.5	397.75	12	90.5
590	S[142]	-656.5	288.25	12	90.5
591	S[143]	-669.5	397.75	12	90.5
592	S[144]	-682.5	288.25	12	90.5
593	S[145]	-695.5	397.75	12	90.5
594	S[146]	-708.5	288.25	12	90.5
595	S[147]	-721.5	397.75	12	90.5
596	S[148]	-734.5	288.25	12	90.5

No.	Name	X-axis	Y-axis	W	H
597	S[149]	-747.5	397.75	12	90.5
598	S[150]	-760.5	288.25	12	90.5
599	S[151]	-773.5	397.75	12	90.5
600	S[152]	-786.5	288.25	12	90.5
601	S[153]	-799.5	397.75	12	90.5
602	S[154]	-812.5	288.25	12	90.5
603	S[155]	-825.5	397.75	12	90.5
604	S[156]	-838.5	288.25	12	90.5
605	S[157]	-851.5	397.75	12	90.5
606	S[158]	-864.5	288.25	12	90.5
607	S[159]	-877.5	397.75	12	90.5
608	S[160]	-890.5	288.25	12	90.5
609	S[161]	-903.5	397.75	12	90.5
610	S[162]	-916.5	288.25	12	90.5
611	S[163]	-929.5	397.75	12	90.5
612	S[164]	-942.5	288.25	12	90.5
613	S[165]	-955.5	397.75	12	90.5
614	S[166]	-968.5	288.25	12	90.5
615	S[167]	-981.5	397.75	12	90.5
616	S[168]	-994.5	288.25	12	90.5
617	S[169]	-1007.5	397.75	12	90.5
618	S[170]	-1020.5	288.25	12	90.5
619	S[171]	-1033.5	397.75	12	90.5
620	S[172]	-1046.5	288.25	12	90.5
621	S[173]	-1059.5	397.75	12	90.5
622	S[174]	-1072.5	288.25	12	90.5
623	S[175]	-1085.5	397.75	12	90.5
624	S[176]	-1098.5	288.25	12	90.5
625	S[177]	-1111.5	397.75	12	90.5
626	S[178]	-1124.5	288.25	12	90.5
627	S[179]	-1137.5	397.75	12	90.5
628	S[180]	-1150.5	288.25	12	90.5
629	S[181]	-1163.5	397.75	12	90.5
630	S[182]	-1176.5	288.25	12	90.5
631	S[183]	-1189.5	397.75	12	90.5
632	DUMMY[42]	-1202.5	288.25	12	90.5
633	DUMMY[43]	-1215.5	397.75	12	90.5
634	DUMMY[44]	-1228.5	288.25	12	90.5
635	DUMMY[45]	-1241.5	397.75	12	90.5
636	DUMMY[46]	-1254.5	288.25	12	90.5
637	DUMMY[47]	-1267.5	397.75	12	90.5
638	DUMMY[48]	-1280.5	288.25	12	90.5
639	DUMMY[49]	-1293.5	397.75	12	90.5
640	VBD2	-1306.5	288.25	12	90.5
641	DUMMY[50]	-1319.5	397.75	12	90.5
642	DUMMY[51]	-1332.5	288.25	12	90.5
643	DUMMY[52]	-1512.5	396.25	12	90.5
644	DUMMY[53]	-1526	286.75	12	90.5
645	DUMMY[54]	-1539.5	396.25	12	90.5
646	DUMMY[55]	-1553	286.75	12	90.5
647	DUMMY[56]	-1566.5	396.25	12	90.5
648	DUMMY[57]	-1580	286.75	12	90.5
649	DUMMY[58]	-1593.5	396.25	12	90.5
650	DUMMY[59]	-1607	286.75	12	90.5
651	DUMMY[60]	-1620.5	396.25	12	90.5
652	DUMMY[61]	-1634	286.75	12	90.5
653	DUMMY[62]	-1647.5	396.25	12	90.5
654	DUMMY[63]	-1661	286.75	12	90.5
655	DUMMY[64]	-1674.5	396.25	12	90.5
656	G[383]	-1688	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
657	G[381]	-1701.5	396.25	12	90.5
658	G[379]	-1715	286.75	12	90.5
659	G[377]	-1728.5	396.25	12	90.5
660	G[375]	-1742	286.75	12	90.5
661	G[373]	-1755.5	396.25	12	90.5
662	G[371]	-1769	286.75	12	90.5
663	G[369]	-1782.5	396.25	12	90.5
664	G[367]	-1796	286.75	12	90.5
665	G[365]	-1809.5	396.25	12	90.5
666	G[363]	-1823	286.75	12	90.5
667	G[361]	-1836.5	396.25	12	90.5
668	G[359]	-1850	286.75	12	90.5
669	G[357]	-1863.5	396.25	12	90.5
670	G[355]	-1877	286.75	12	90.5
671	G[353]	-1890.5	396.25	12	90.5
672	G[351]	-1904	286.75	12	90.5
673	G[349]	-1917.5	396.25	12	90.5
674	G[347]	-1931	286.75	12	90.5
675	G[345]	-1944.5	396.25	12	90.5
676	G[343]	-1958	286.75	12	90.5
677	G[341]	-1971.5	396.25	12	90.5
678	G[339]	-1985	286.75	12	90.5
679	G[337]	-1998.5	396.25	12	90.5
680	G[335]	-2012	286.75	12	90.5
681	G[333]	-2025.5	396.25	12	90.5
682	G[331]	-2039	286.75	12	90.5
683	G[329]	-2052.5	396.25	12	90.5
684	G[327]	-2066	286.75	12	90.5
685	G[325]	-2079.5	396.25	12	90.5
686	G[323]	-2093	286.75	12	90.5
687	G[321]	-2106.5	396.25	12	90.5
688	G[319]	-2120	286.75	12	90.5
689	G[317]	-2133.5	396.25	12	90.5
690	G[315]	-2147	286.75	12	90.5
691	G[313]	-2160.5	396.25	12	90.5
692	G[311]	-2174	286.75	12	90.5
693	G[309]	-2187.5	396.25	12	90.5
694	G[307]	-2201	286.75	12	90.5
695	G[305]	-2214.5	396.25	12	90.5
696	G[303]	-2228	286.75	12	90.5
697	G[301]	-2241.5	396.25	12	90.5
698	G[299]	-2255	286.75	12	90.5
699	G[297]	-2268.5	396.25	12	90.5
700	G[295]	-2282	286.75	12	90.5
701	G[293]	-2295.5	396.25	12	90.5
702	G[291]	-2309	286.75	12	90.5
703	G[289]	-2322.5	396.25	12	90.5
704	G[287]	-2336	286.75	12	90.5
705	G[285]	-2349.5	396.25	12	90.5
706	G[283]	-2363	286.75	12	90.5
707	G[281]	-2376.5	396.25	12	90.5
708	G[279]	-2390	286.75	12	90.5
709	G[277]	-2403.5	396.25	12	90.5
710	G[275]	-2417	286.75	12	90.5
711	G[273]	-2430.5	396.25	12	90.5
712	G[271]	-2444	286.75	12	90.5
713	G[269]	-2457.5	396.25	12	90.5
714	G[267]	-2471	286.75	12	90.5
715	G[265]	-2484.5	396.25	12	90.5
716	G[263]	-2498	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
717	G[261]	-2511.5	396.25	12	90.5
718	G[259]	-2525	286.75	12	90.5
719	G[257]	-2538.5	396.25	12	90.5
720	G[255]	-2552	286.75	12	90.5
721	G[253]	-2565.5	396.25	12	90.5
722	G[251]	-2579	286.75	12	90.5
723	G[249]	-2592.5	396.25	12	90.5
724	G[247]	-2606	286.75	12	90.5
725	G[245]	-2619.5	396.25	12	90.5
726	G[243]	-2633	286.75	12	90.5
727	G[241]	-2646.5	396.25	12	90.5
728	G[239]	-2660	286.75	12	90.5
729	G[237]	-2673.5	396.25	12	90.5
730	G[235]	-2687	286.75	12	90.5
731	G[233]	-2700.5	396.25	12	90.5
732	G[231]	-2714	286.75	12	90.5
733	G[229]	-2727.5	396.25	12	90.5
734	G[227]	-2741	286.75	12	90.5
735	G[225]	-2754.5	396.25	12	90.5
736	G[223]	-2768	286.75	12	90.5
737	G[221]	-2781.5	396.25	12	90.5
738	G[219]	-2795	286.75	12	90.5
739	G[217]	-2808.5	396.25	12	90.5
740	G[215]	-2822	286.75	12	90.5
741	G[213]	-2835.5	396.25	12	90.5
742	G[211]	-2849	286.75	12	90.5
743	G[209]	-2862.5	396.25	12	90.5
744	G[207]	-2876	286.75	12	90.5
745	G[205]	-2889.5	396.25	12	90.5
746	G[203]	-2903	286.75	12	90.5
747	G[201]	-2916.5	396.25	12	90.5
748	G[199]	-2930	286.75	12	90.5
749	G[197]	-2943.5	396.25	12	90.5
750	G[195]	-2957	286.75	12	90.5
751	G[193]	-2970.5	396.25	12	90.5
752	G[191]	-2984	286.75	12	90.5
753	G[189]	-2997.5	396.25	12	90.5
754	G[187]	-3011	286.75	12	90.5
755	G[185]	-3024.5	396.25	12	90.5
756	G[183]	-3038	286.75	12	90.5
757	G[181]	-3051.5	396.25	12	90.5
758	G[179]	-3065	286.75	12	90.5
759	G[177]	-3078.5	396.25	12	90.5
760	G[175]	-3092	286.75	12	90.5
761	G[173]	-3105.5	396.25	12	90.5
762	G[171]	-3119	286.75	12	90.5
763	G[169]	-3132.5	396.25	12	90.5
764	G[167]	-3146	286.75	12	90.5
765	G[165]	-3159.5	396.25	12	90.5
766	G[163]	-3173	286.75	12	90.5
767	G[161]	-3186.5	396.25	12	90.5
768	G[159]	-3200	286.75	12	90.5
769	G[157]	-3213.5	396.25	12	90.5
770	G[155]	-3227	286.75	12	90.5
771	G[153]	-3240.5	396.25	12	90.5
772	G[151]	-3254	286.75	12	90.5
773	G[149]	-3267.5	396.25	12	90.5
774	G[147]	-3281	286.75	12	90.5
775	G[145]	-3294.5	396.25	12	90.5
776	G[143]	-3308	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
777	G[141]	-3321.5	396.25	12	90.5
778	G[139]	-3335	286.75	12	90.5
779	G[137]	-3348.5	396.25	12	90.5
780	G[135]	-3362	286.75	12	90.5
781	G[133]	-3375.5	396.25	12	90.5
782	G[131]	-3389	286.75	12	90.5
783	G[129]	-3402.5	396.25	12	90.5
784	G[127]	-3416	286.75	12	90.5
785	G[125]	-3429.5	396.25	12	90.5
786	G[123]	-3443	286.75	12	90.5
787	G[121]	-3456.5	396.25	12	90.5
788	G[119]	-3470	286.75	12	90.5
789	G[117]	-3483.5	396.25	12	90.5
790	G[115]	-3497	286.75	12	90.5
791	G[113]	-3510.5	396.25	12	90.5
792	G[111]	-3524	286.75	12	90.5
793	G[109]	-3537.5	396.25	12	90.5
794	G[107]	-3551	286.75	12	90.5
795	G[105]	-3564.5	396.25	12	90.5
796	G[103]	-3578	286.75	12	90.5
797	G[101]	-3591.5	396.25	12	90.5
798	G[99]	-3605	286.75	12	90.5
799	G[97]	-3618.5	396.25	12	90.5
800	G[95]	-3632	286.75	12	90.5
801	G[93]	-3645.5	396.25	12	90.5
802	G[91]	-3659	286.75	12	90.5
803	G[89]	-3672.5	396.25	12	90.5
804	G[87]	-3686	286.75	12	90.5
805	G[85]	-3699.5	396.25	12	90.5
806	G[83]	-3713	286.75	12	90.5
807	G[81]	-3726.5	396.25	12	90.5
808	G[79]	-3740	286.75	12	90.5
809	G[77]	-3753.5	396.25	12	90.5
810	G[75]	-3767	286.75	12	90.5
811	G[73]	-3780.5	396.25	12	90.5
812	G[71]	-3794	286.75	12	90.5
813	G[69]	-3807.5	396.25	12	90.5
814	G[67]	-3821	286.75	12	90.5
815	G[65]	-3834.5	396.25	12	90.5
816	G[63]	-3848	286.75	12	90.5
817	G[61]	-3861.5	396.25	12	90.5
818	G[59]	-3875	286.75	12	90.5
819	G[57]	-3888.5	396.25	12	90.5
820	G[55]	-3902	286.75	12	90.5
821	G[53]	-3915.5	396.25	12	90.5
822	G[51]	-3929	286.75	12	90.5
823	G[49]	-3942.5	396.25	12	90.5
824	G[47]	-3956	286.75	12	90.5
825	G[45]	-3969.5	396.25	12	90.5
826	G[43]	-3983	286.75	12	90.5
827	G[41]	-3996.5	396.25	12	90.5
828	G[39]	-4010	286.75	12	90.5
829	G[37]	-4023.5	396.25	12	90.5
830	G[35]	-4037	286.75	12	90.5
831	G[33]	-4050.5	396.25	12	90.5
832	G[31]	-4064	286.75	12	90.5
833	G[29]	-4077.5	396.25	12	90.5
834	G[27]	-4091	286.75	12	90.5
835	G[25]	-4104.5	396.25	12	90.5
836	G[23]	-4118	286.75	12	90.5

No.	Name	X-axis	Y-axis	W	H
837	G[21]	-4131.5	396.25	12	90.5
838	G[19]	-4145	286.75	12	90.5
839	G[17]	-4158.5	396.25	12	90.5
840	G[15]	-4172	286.75	12	90.5
841	G[13]	-4185.5	396.25	12	90.5
842	G[11]	-4199	286.75	12	90.5
843	G[9]	-4212.5	396.25	12	90.5
844	G[7]	-4226	286.75	12	90.5
845	G[5]	-4239.5	396.25	12	90.5
846	G[3]	-4253	286.75	12	90.5
847	G[1]	-4266.5	396.25	12	90.5
848	T_LDON5V	-4280	286.75	12	90.5
849	T_LDON5V	-4293.5	396.25	12	90.5
850	T_VCOM	-4307	286.75	12	90.5
851	T_VCOM	-4320.5	396.25	12	90.5
852	T_N18V	-4334	286.75	12	90.5
853	T_N18V	-4347.5	396.25	12	90.5
854	DUMMY[65]	-4361	286.75	12	90.5
855	DUMMY[66]	-4374.5	396.25	12	90.5
856	DUMMY[67]	-4388	286.75	12	90.5
857	DUMMY[68]	-4401.5	396.25	12	90.5
858	DUMMY[69]	-4415	286.75	12	90.5
859	DUMMY[70]	-4428.5	396.25	12	90.5
860	DUMMY[84]	-4462	396.25	12	90.5
861	DUMMY[85]	-4502	396.25	12	90.5
862	DUMMY[86]	-4542	396.25	12	90.5
863	DUMMY[87]	-4582	396.25	12	90.5
864	DUMMY[88]	-4730	286.75	12	90.5
865	DUMMY[89]	-4770	286.75	12	90.5
866	DUMMY[90]	-4810	286.75	12	90.5

13. REVISION HISTORY

Revision	Content	Page	Date
1.0.1	JD79667AA datasheet	-	2023/06/14
1.0.2	Updated Bump information		2023/06/14
1.0.3	Updated Bump information		2023/06/20
1.0.4	Modify application circuit BS pin (must tie high or low)		2023/07/20