JADARD

JD79668AA

Data Sheet

All-in-one driver with
TCON for Color application

Version 1.0.4
2023/06/20

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1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 2-bit output per pixel. The timing controller provides control signals for the source driver and gate drivers.

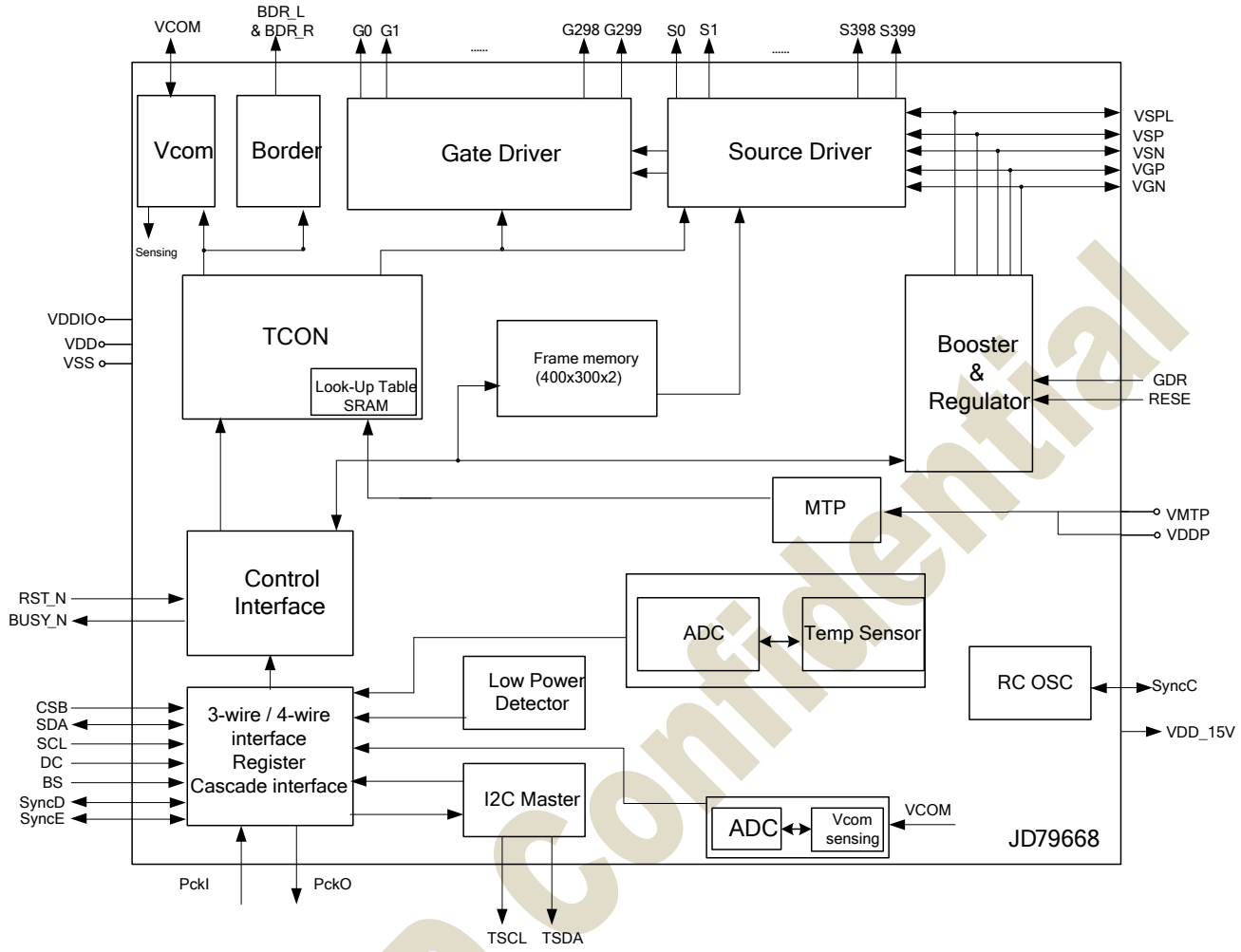
The DC-DC controller allows to generate the source output voltage VSP_0/VSN_0(+/-15V),VSP_1/VSPL_0/VSPL_1/VSN_1 (+/-3V~+/-15V) and VGP/VGN(+/-20V, +/-17V, +/-15V, +/-10V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire(SPI) serial.

2. FEATURES

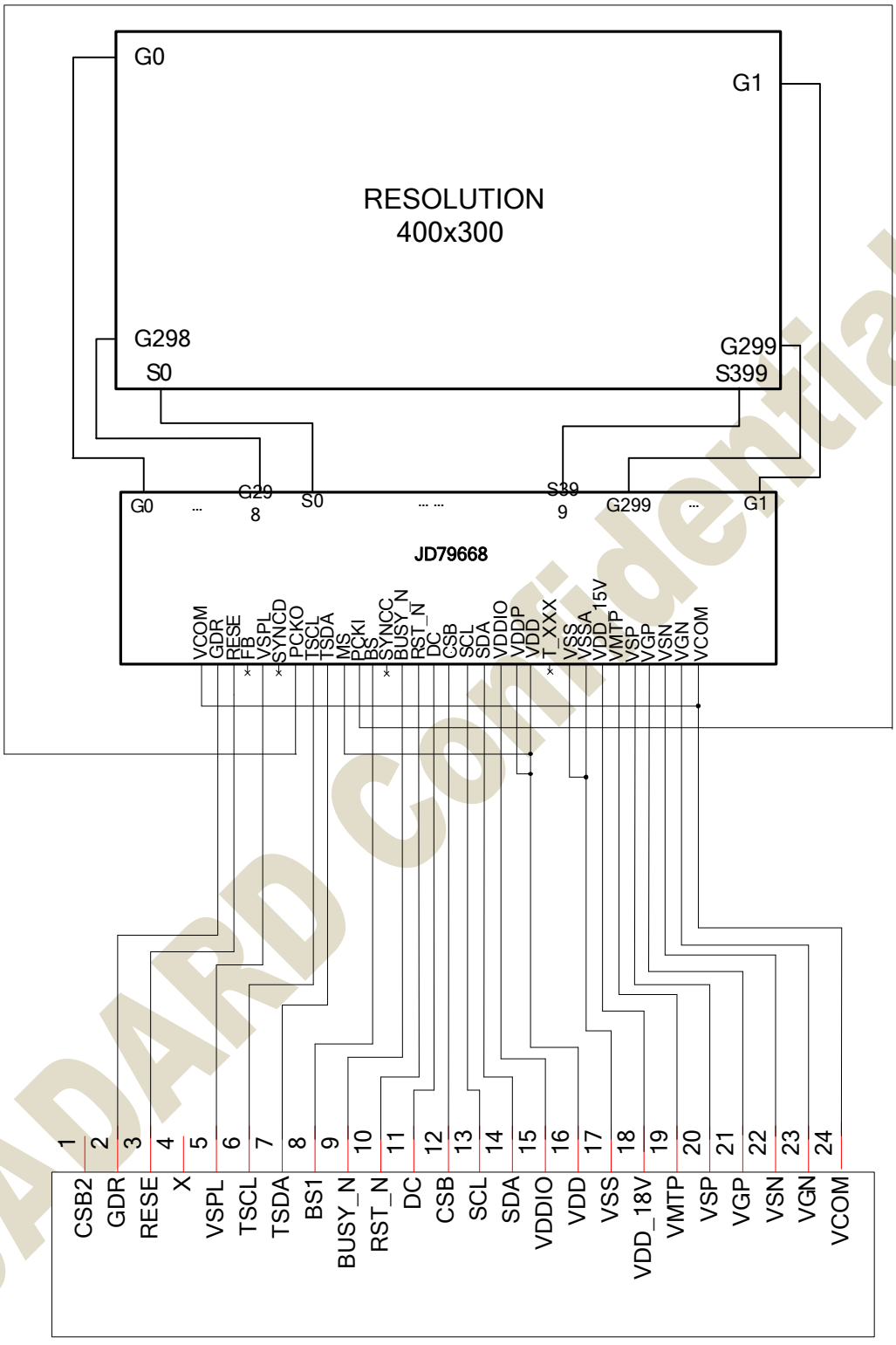
- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 400x300)
- Support source & gate driver function:
  - 400 Outputs source driver with 2-bit black/white/red/yellow per pixel:
    - Output dynamic range(Voltage step:100mV):
      - Mode 0: 0V & VSP_0(+15V) & VSN_0(-15V) & VSPL_0(+3V~+15V)
      - Mode 1: 0V & VSP_1 (+3V ~ +15V) & VSN_1(-3V ~ -15V) & VSPL_1 (+3V ~ +15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 300 Output gate driver:
    - Output dynamic range: VGP and VGN(+/-20V, +/-17V, +/-15V, +/-10V)
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (7-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: 400 x 300 x 2 bit SRAM
- Built in temperature sensor:
  - On-Chip: -25 ^{o}C ~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V
- 4.0 K-byte MTP for LUT, User command
- Partial update

- Support cascade
- Package-COG

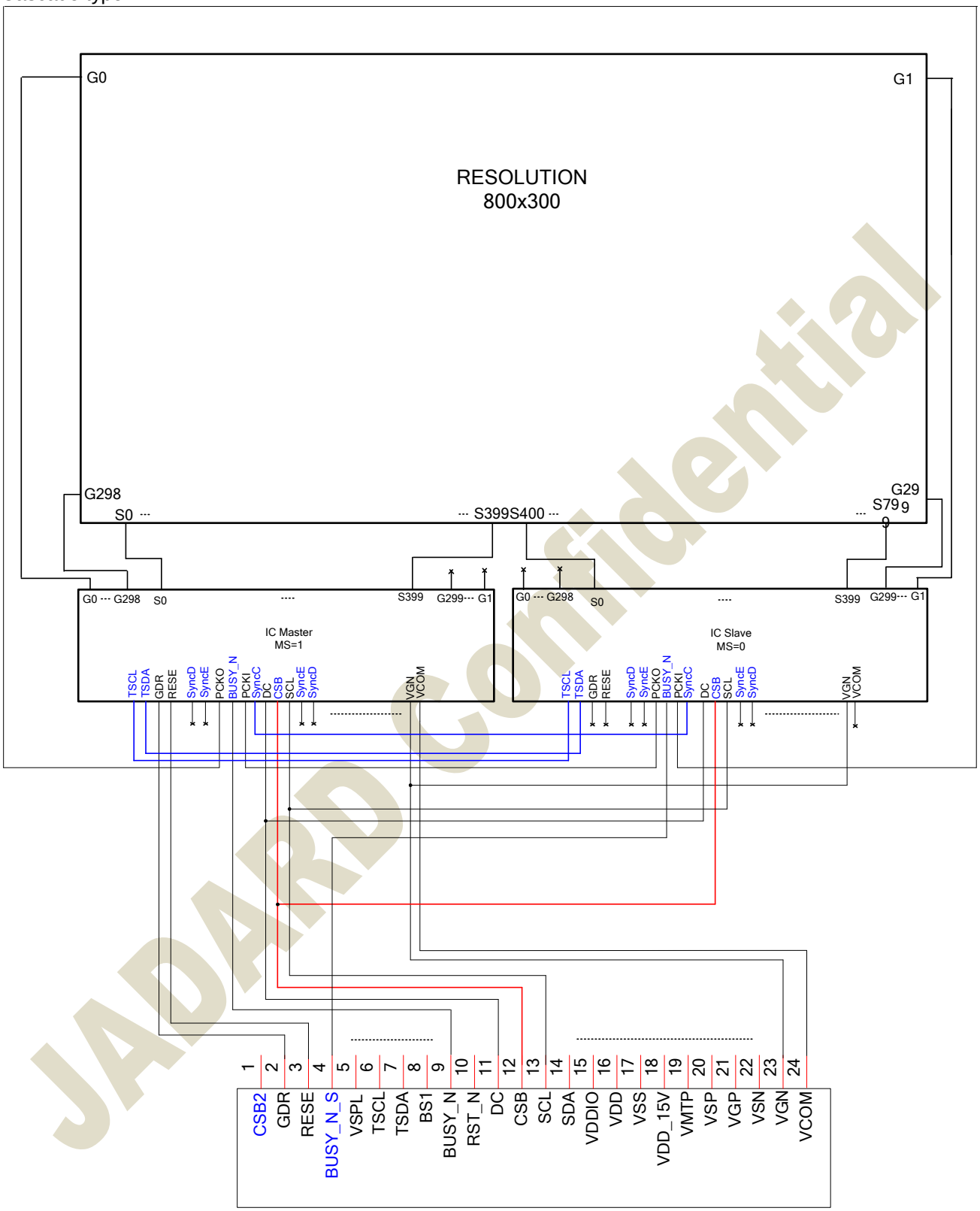
3. BLOCK DIAGRAM



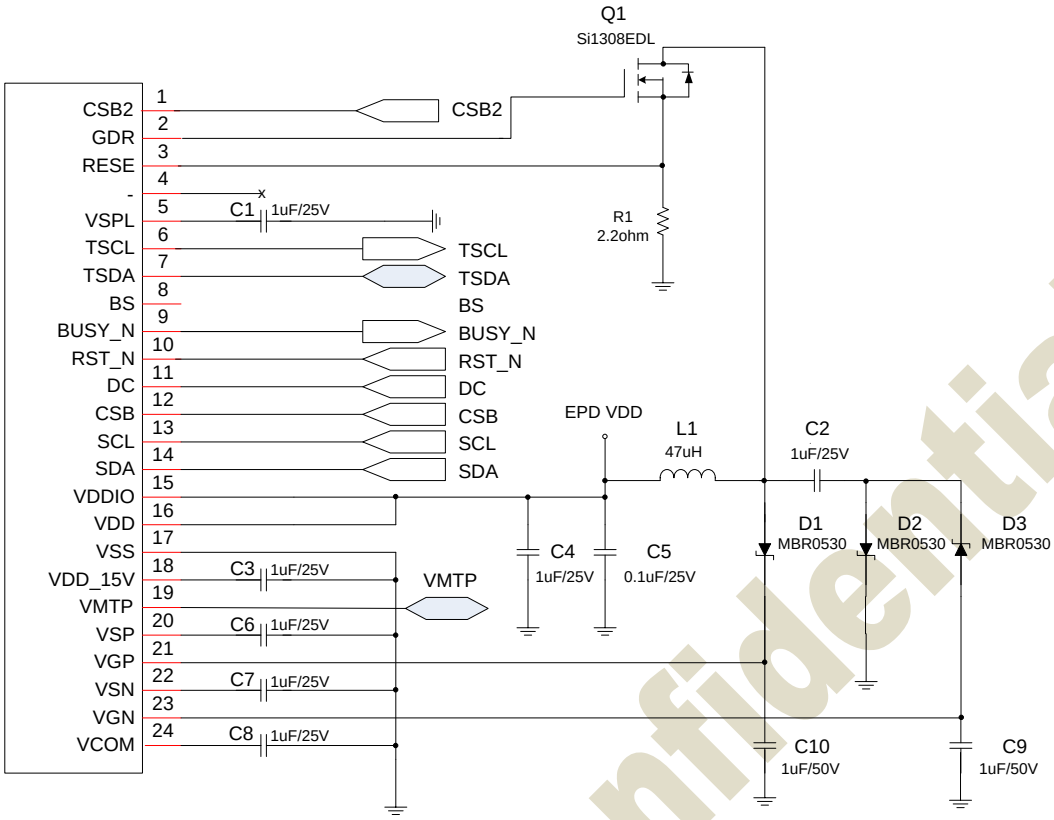
Normal type

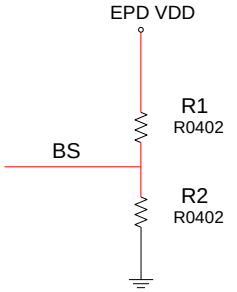


Cascade type



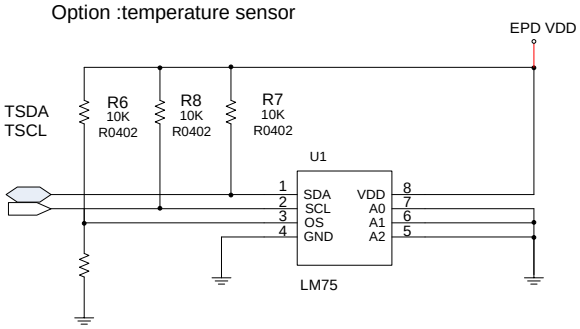
4. APPLICATION CIRCUIT





	R1	R2
3- wire SPI (CSB, SDA, SCL)	10K	NC
4-wire SPI (DC, CSB, SDA, SCL)	NC	10K

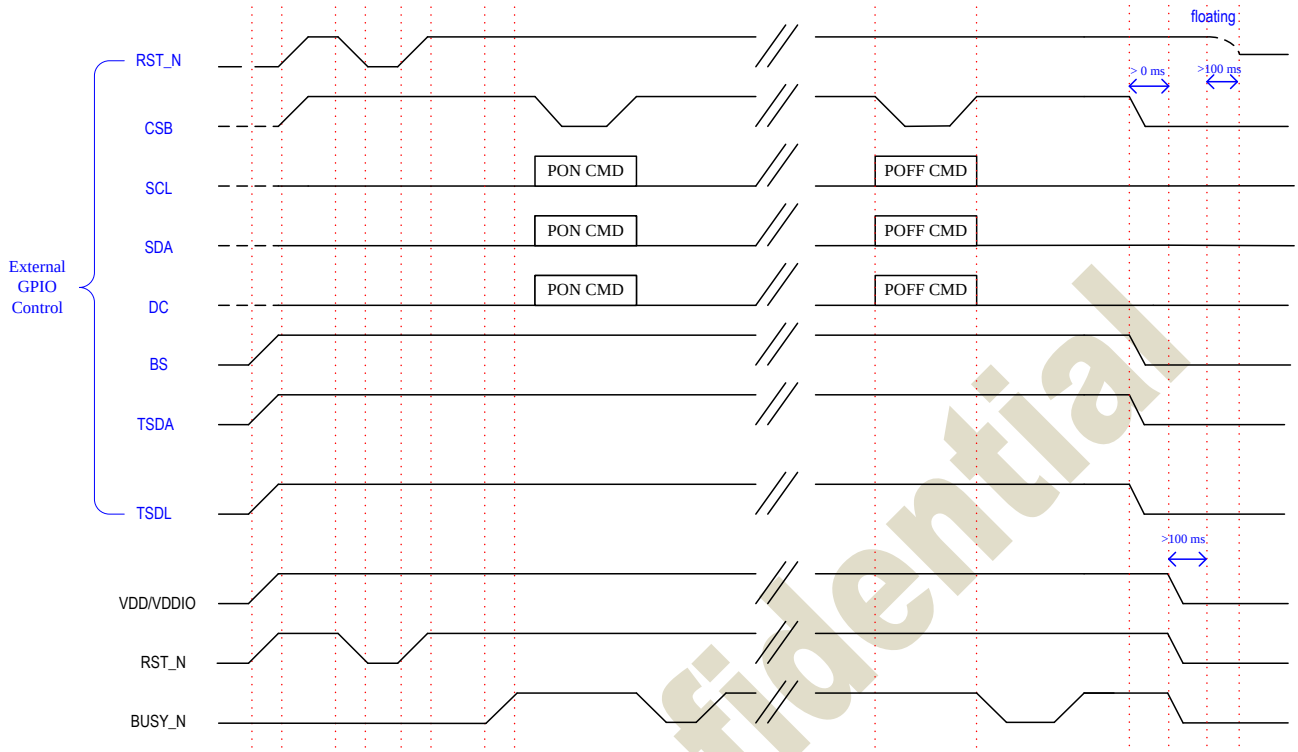
Option :temperature sensor



Reference table of the device:

Device no.	Value	Reference
C1,C2,C3, C4, C6, C7, C8	1uF	0603, X5R/X7R, voltage rating : 25V
C9, C10	1uF	0603, X5R/X7R, voltage rating : 50V
C5	0.1uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47uH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ
D1~D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV

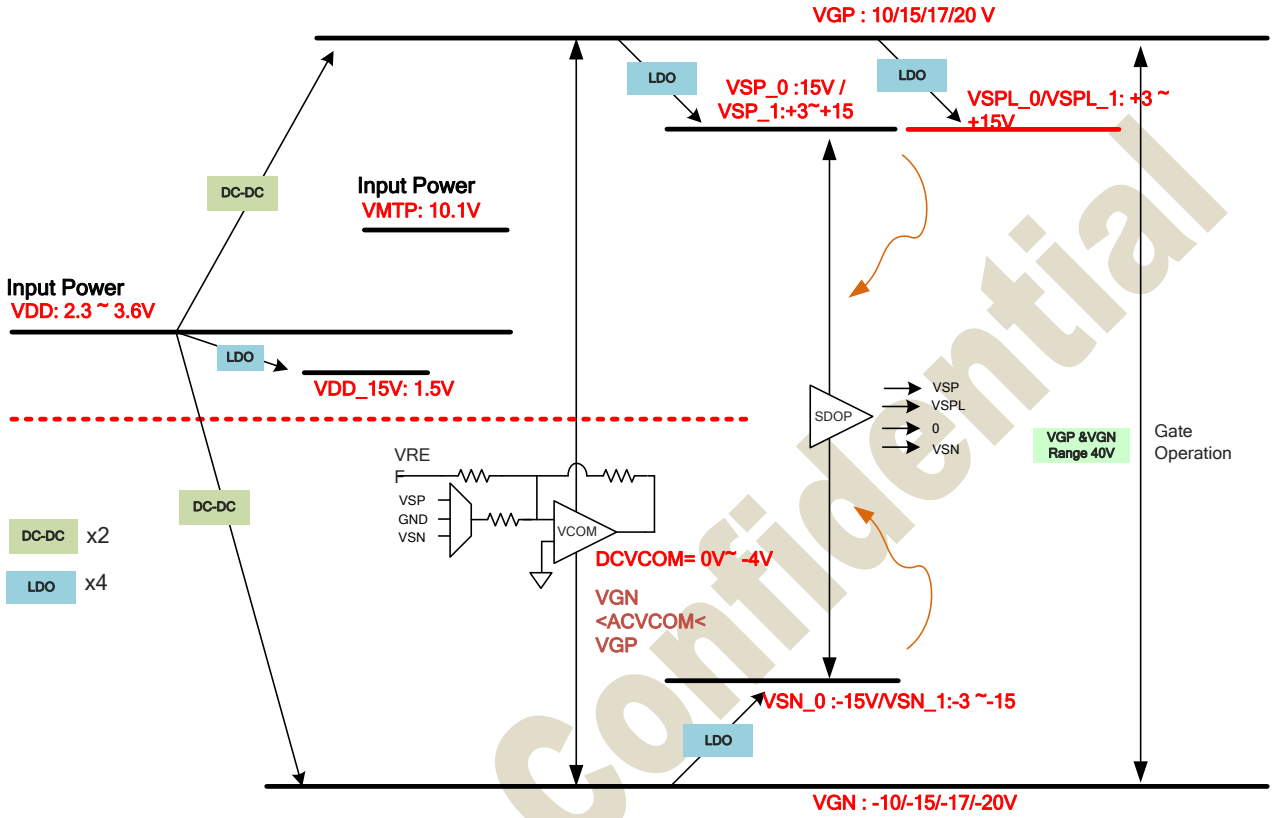
4.1 External GPIO Control



Note:
TSDA: I^2C data for external temperature sensor
TSCL: I^2C clock for external temperature sensor
(I^2C interface need external pull high resistance. Pull low or floating If not used.)

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

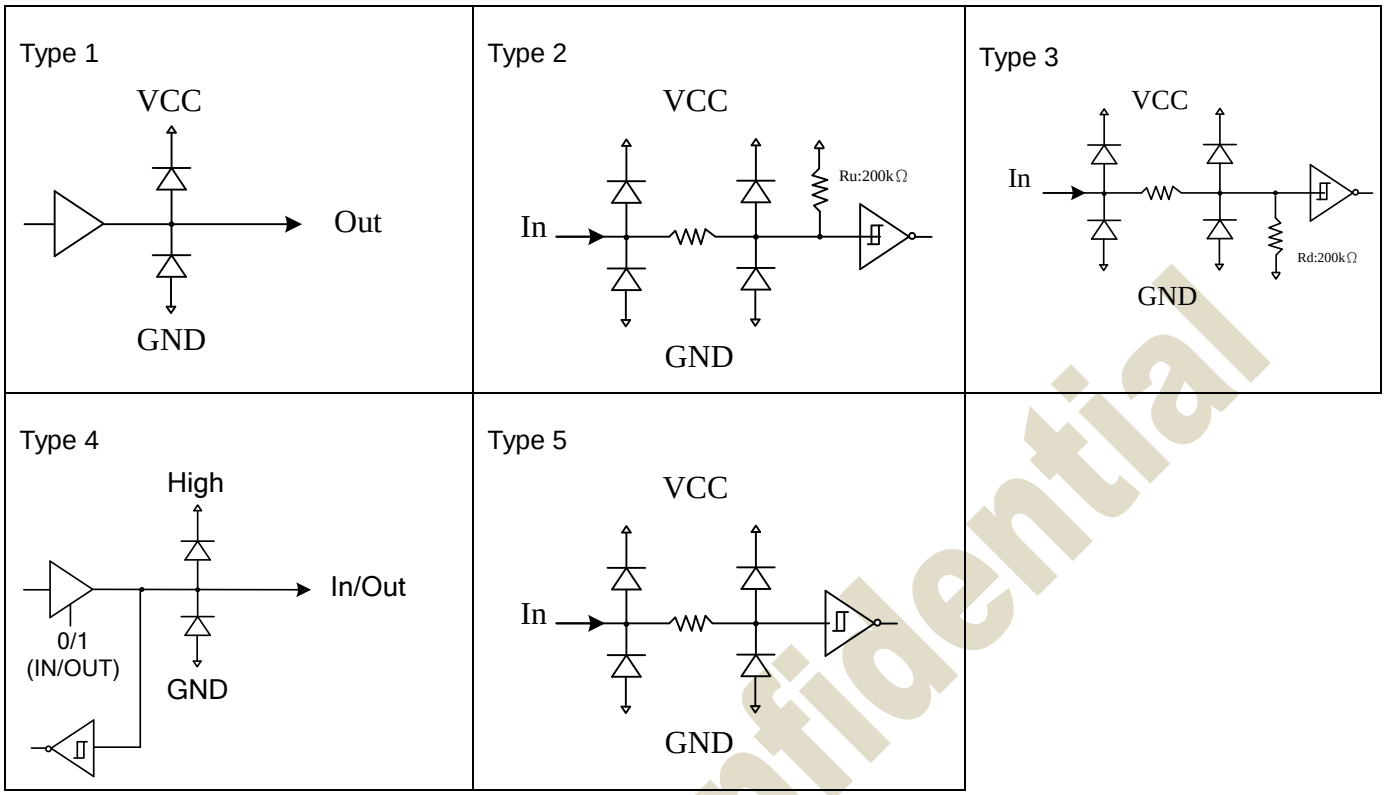
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. (normal pull high) When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF
TSCL	I/O	Type 4	I^2C clock for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used. (Default low)
TSDA	I/O	Type 4	I^2C data for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[399:0]	O	-	Source driver output signals.
G[299:0]	O	-	Gate driver output signals..
Border			
VBD[2:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) V 2. (15 +(- VCM_DC)) V or (-15 +(- VCM_DC)) V 3. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGP	P		Positive gate voltage
VGN	P	-	Negative gate voltage.
VSP	P	-	Positive source voltage
VSN	P	-	Negative source voltage.
VSPL	P	-	Positive source voltage

Pin Name	Pin Type	I/O Structure	Description
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_15V	P	-	1.5V voltage input &output
VMTP	P	-	MTP program power (10.1V)
Reserved Pins			
T_N18V	I/O	-	Test pin.Leave open or pull gnd.
T_LDON5V	I/O	-	Test pin.Leave open or pull gnd.
T_VCOM	I/O	-	Test pin.Leave open or pull gnd.
T_VSPD_REF	I/O	-	Test pin.Leave open or pull gnd.
T_IBIAS	I/O	-	Test pin.Leave open or pull gnd.
T_VREF	I/O	-	Test pin.Leave open or pull gnd.
T_EN_LSH	I/O	-	Test pin.Leave open or pull gnd.
T_VTSEN	I/O	-	Test pin.Leave open or pull gnd.
T_SAR_REF	I/O	-	Test pin.Leave open or pull gnd.
T_IN[2:0]	I/O	-	Test pin.Leave open or pull gnd.
T_DEBUG[8:0]	I/O	-	Test pin.Leave open or pull gnd.
T_EX_SYSCLK	I/O	-	Test pin.Leave open or pull gnd.
T_EX_REFCLK	I/O	-	Test pin.Leave open or pull gnd.
T_EN_DIG	I/O	-	Test pin.Leave open or pull gnd.
SyncD	I/O	Type 4	Cascade data signal. Leave open or pull gnd if it is not used.
SyncE	I/O	Type 4	Cascade data2 signal. Leave open or pull gnd if it is not used.
SyncC	I/O	Type 4	Cascade clock signal. Leave open or pull gnd if it is not used.
PckI	I	Type 3	Break panel check input. Leave open or gnd if it is not used.
PckO	O	Type 1	Break panel check output. Leave open or gnd if it is not used.
DUMMY[91:0]	D	-	Dummy pin. Leave open or pull gnd.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGP	5ohm	TSCL	100ohm
VGN	5ohm	BS	100ohm
VSP	5ohm	RESE	5ohm
VSN	5ohm	GDR	5ohm
VSPL	5ohm	SDA	100ohm
VMTP	5ohm	SCL	100ohm
VDD_15V	5ohm	CSB	100ohm
VSSA	5ohm	DC	100ohm
VDDIO	5ohm	RST_N	100ohm
VSS	5ohm	SyncD	100ohm
VDDP	5ohm	SyncE	100ohm
VDD	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
Test pin	100ohm	PCKO	100ohm
BUSY_N	100ohm		

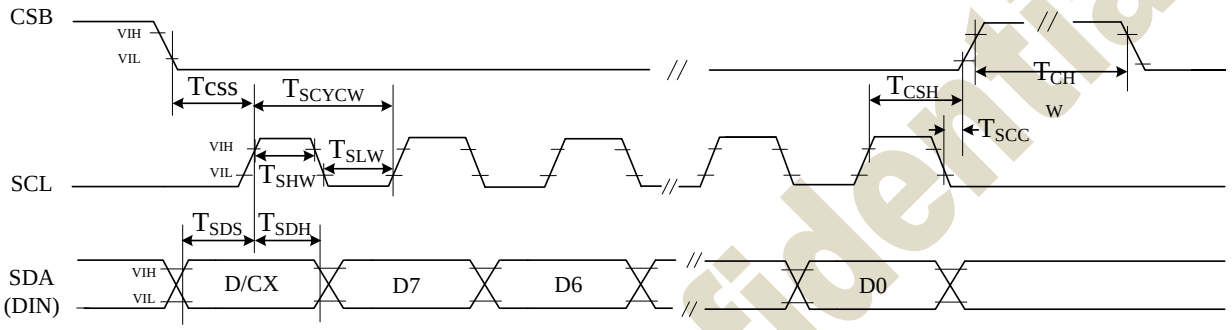
7. SPI COMMAND DESCRIPTION

JD79668 use the 3-wire/4-wire serial port as communication interface for all the function and command setting.

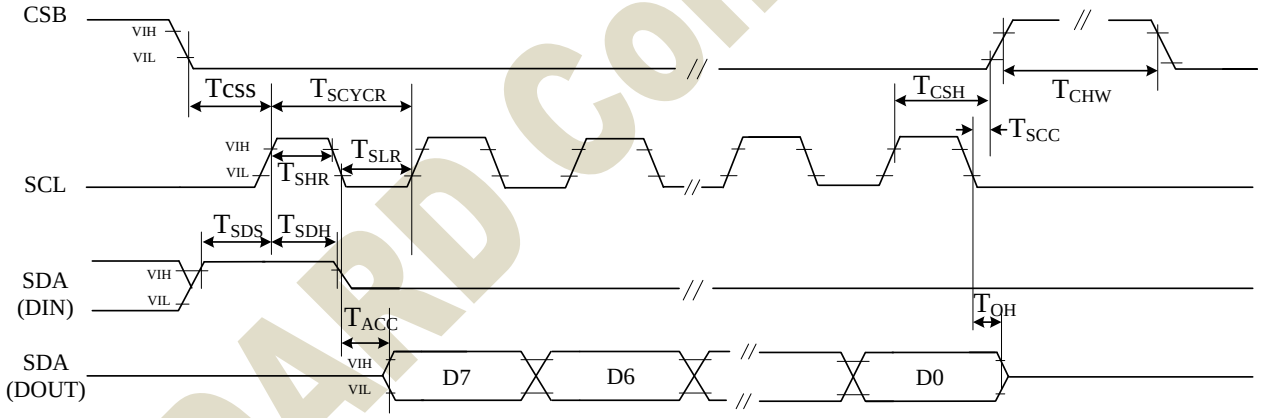
JD79668 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

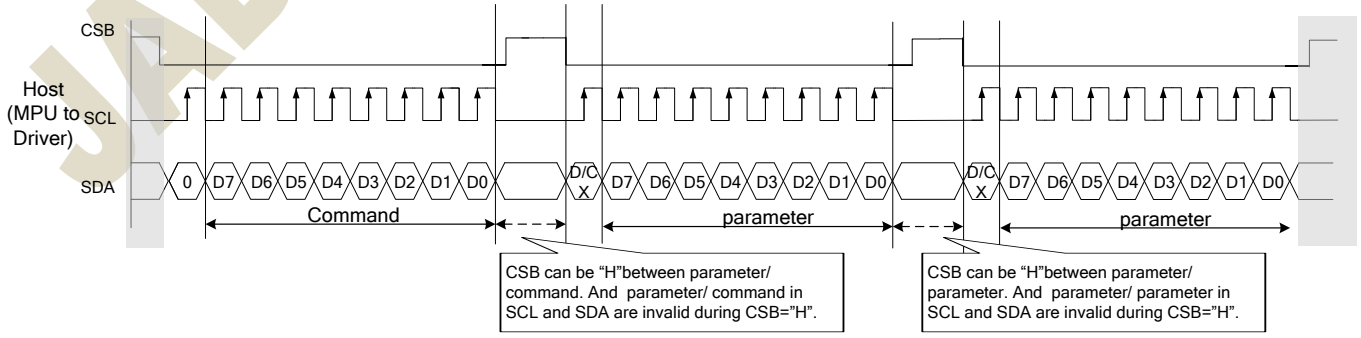
7.1 “3-Wire” Serial Port Interface



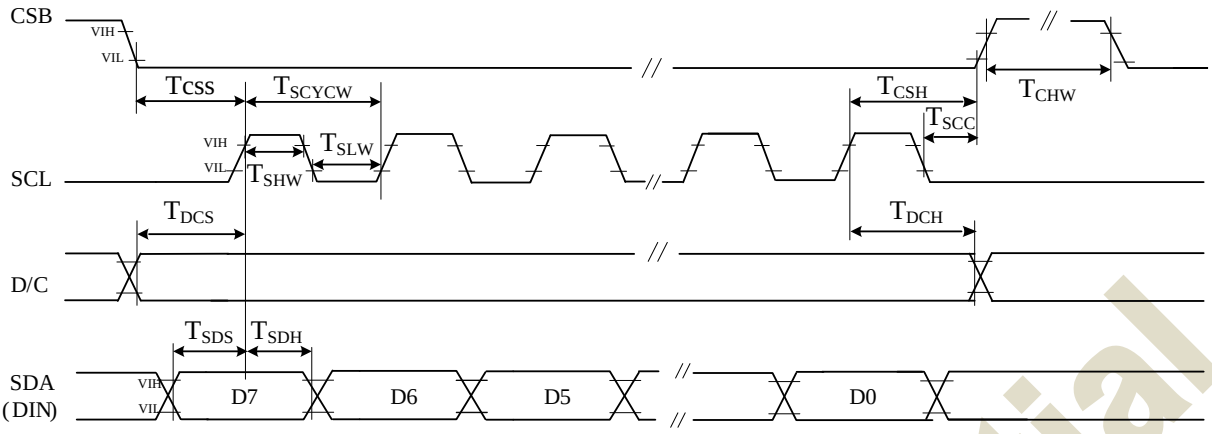
3 pin serial interface characteristics (write mode)



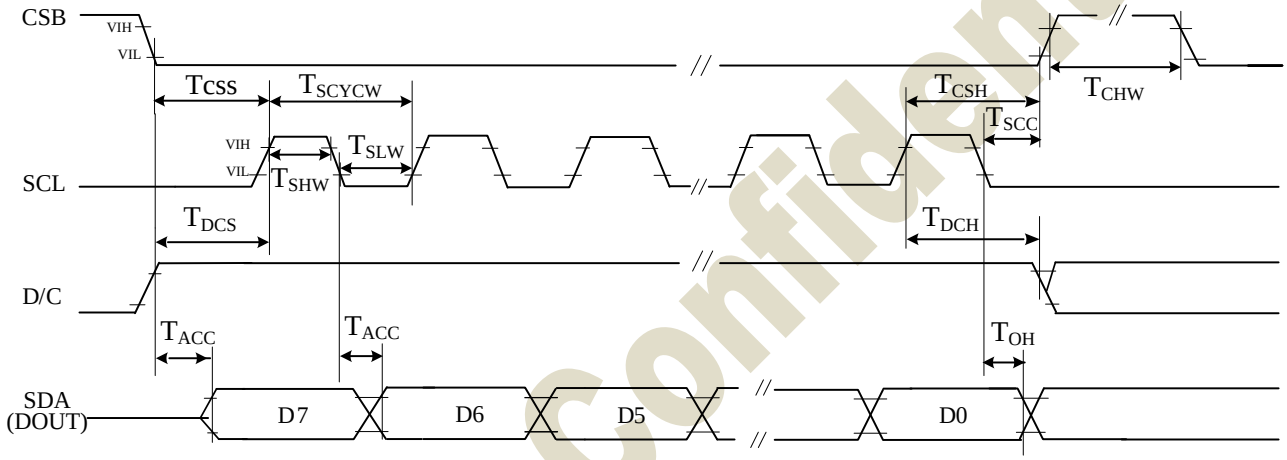
3 pin serial interface characteristics (read mode)



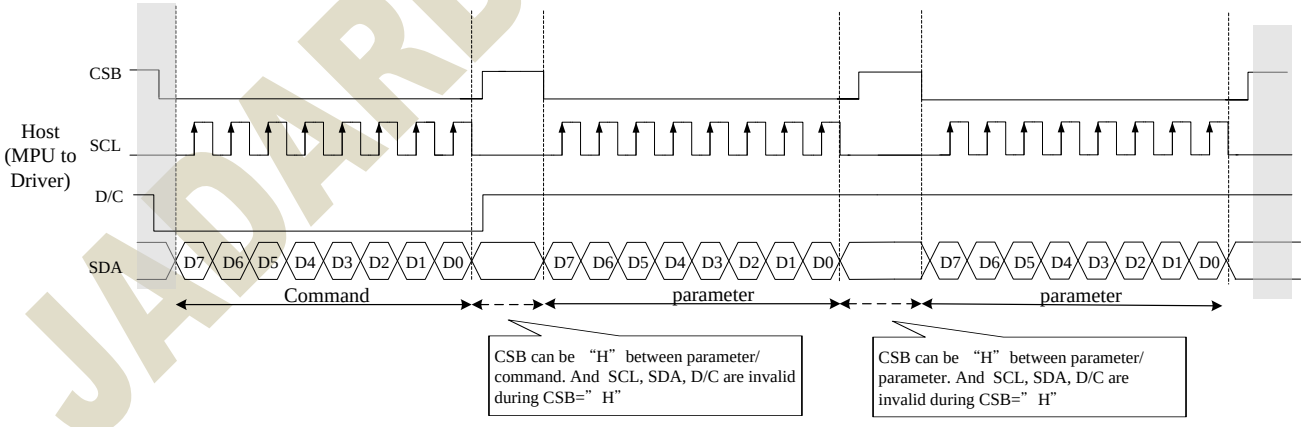
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79668. Refer to the next section for detail register function description.

Address	command			Bit								
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-		-	-	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	PHA_ON[5:0]						02h
		W	1	-	-	PHA_OFF[5:0]						07h
		W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	00H
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna		FR[2:0]		02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/ TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--

R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	gscan	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	0	0	1	1	06h
		R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	01h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	PTH_ENB	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMODE	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
RA2H	MTP Program Config Register(PGM_CFG)	W	0	1	0	1	0	0	0	1	0	A2H
		W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
		W	1	PGM_SADDR[15:8]								00h
		W	1	PGM_SADDR[7:0]								00h
		W	1	PGM_DSIZE[15:8]								0Fh
		W	1	PGM_DSIZE[7:0]								00h
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	-	-	-	CCEIN	00h
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h

8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source / Border / Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 400x300(default) 01: Display resolution is 320x300 10: Display resolution is 300x240 11: Display resolution is 200x300

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display, the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction	

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	**Internal VSP & VSPL power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	**Internal VSN power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
   I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	+10v	+10v
	VGN	-10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)= -10 v
	VCOMDC	-2v	-2v

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R02h = 0x00h ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.2.4R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence (base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.2.5 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
	000001	Period2	010111	Period24	101101	Period46
	000010	Period3	011000	Period25	101110	Period47
	000011	Period4	011001	Period26	101111	Period48
	000100	Period5	011010	Period27	110000	Period49
	000101	Period6	011011	Period28	110001	Period50
	000110	Period7	011100	Period29	110010	Period51
	000111	Period8	011101	Period30	110011	Period52
	001000	Period9	011110	Period31	110100	Period53
	001001	Period10	011111	Period32	110101	Period54
	001010	Period11	100000	Period33	110110	Period55
	001011	Period12	100001	Period34	110111	Period56
	001100	Period13	100010	Period35	111000	Period57
	001101	Period14	100011	Period36	111001	Period58
	001110	Period15	100100	Period37	111010	Period59
	001111	Period16	100101	Period38	111011	Period60
	010000	Period17	100110	Period39	111100	Period61
	010001	Period18	100111	Period40	111101	Period62
	010010	Period19	101000	Period41	111110	Period63
	010011	Period20	101001	Period42	111111	Period64
	010100	Period21	101010	Period43		
	010101	Period22	101011	Period44		

Restriction

8.2.6 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.2.7 R10H (DTM): Data Start transmission Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM_master	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
:	W	1	:		:		:		:		00h
Mth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.

Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1,Pixel[1:0]=01 ->Gray level select=Gray1,follow LUT data output from IP output port"ogray01".

When DDX=0,Pixel[1:0]=11 ->Gray level select=Gray0,follow LUT data output from IP output port"ogray00"

Restriction

8.2.8 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

- While finished the data transmitting, user must send this command to driver and read Data_flag information.

1st Parameter:

Bit	Name	Description
7	Data_flag	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.

After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

Restriction

This command only actives when BUSY_N = "1".

8.2.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R12H=0x00 While users send this command, driver will refresh display base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

8.2.10 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

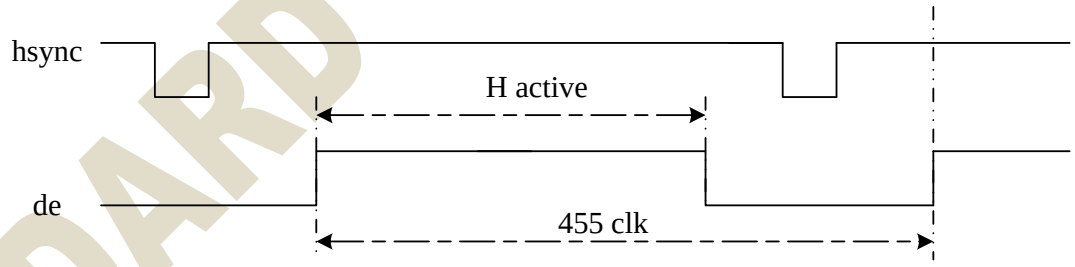
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

bit3	Dynamic frame rate
0	Disable(default)
1	Enable

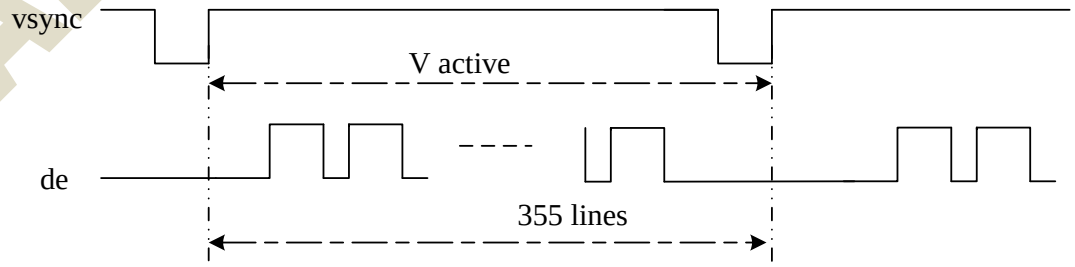
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



Restriction

8.2.12 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

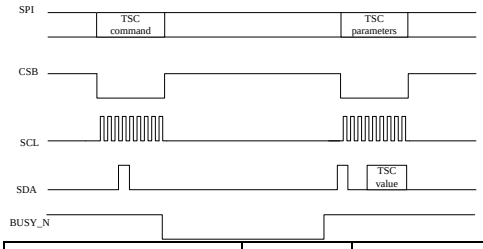
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[9:8]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

8.2.13 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +0.5℃ 0010: +1℃ 0011: +1.5℃ 0100: +2℃ 0101: +2.5℃ 0110: +3℃ 0111: +3.5℃ 1000: -4℃ 1001: -3.5℃ 1010: -3℃ 1011: -2.5℃ 1100: -2℃ 1101: -1.5℃ 1110: -1℃ 1111: -0.5℃
4	TO[4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

8.2.14 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction: This command only actives after R04H(PON)

8.2.15 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

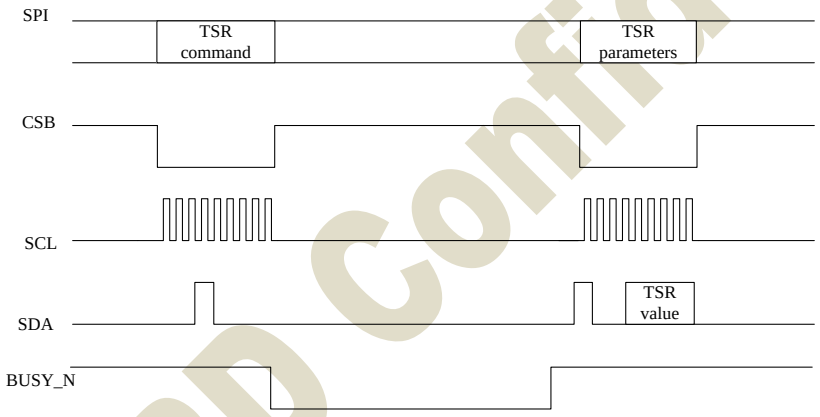
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction: This command only actives after R04H(PON)

8.2.16 R50H (CDI): VCOM and DATA interval setting Register

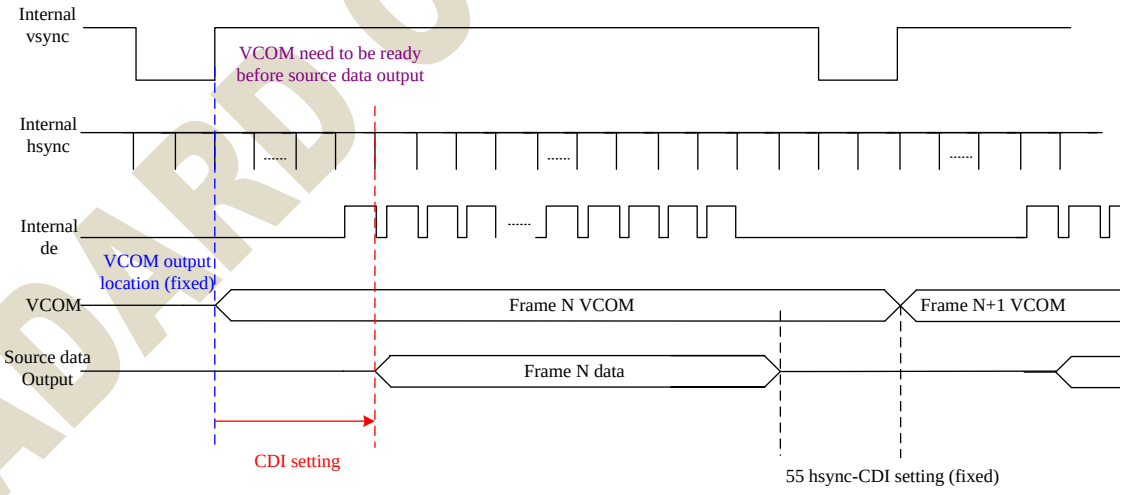
R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)
:
CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.

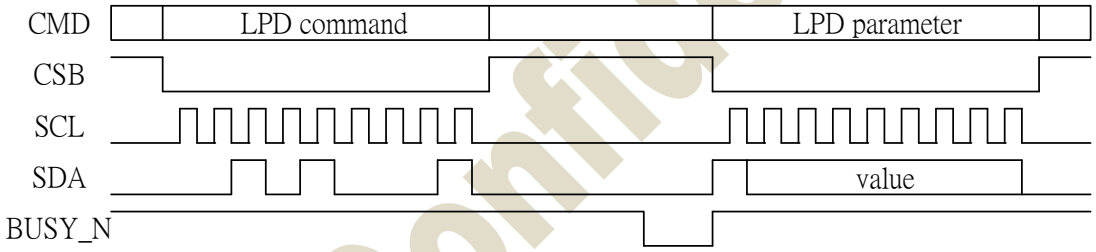
Boarder output will follow FOPT definition being defined in R00h.

Restriction	

8.2.17 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)). 1st Parameter: Bit 0 / LPD 0 / Low power input. 1 / Normal status. 
Restriction	This command only actives when BUSY_N = "1".

8.2.18 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3th Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Note: No matter HRES[9],HRES[1:0],VRES[9] value being filled, it's always be 00b. Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1 EX :400X300 GD: First G active = G0 LAST active GD= 0+300-1= 299; (G299) SD : First active channel: =S0 LAST active SD=0+100*4-1=399; (S399)
Restriction	Horizontal resolution should be 4-multiple.

8.2.19 R65H (GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3rd Parameter	W	1	-	-	-	gscan	-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

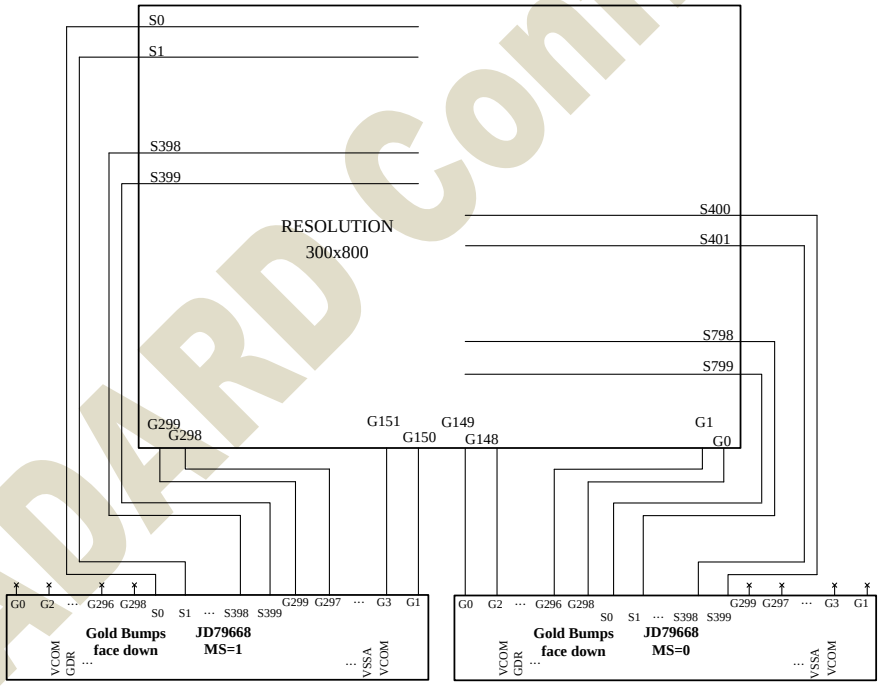
Description

-The command define as follows:

Note:
No matter S_start[9], S_start [1:0],G_start[9] value being filled, it's always be 00b.

1.S_Start [8:0] describe which source output line is the first date line
2.G_Start[8:0] describe which gate line is the first scan line
3. gscan :Gate scan select
0: Normal scan(default)
1: Cascade type scan

Scanning mode setting (gscan=1): 800x300



Restriction

S_Start should be the multiple of 4

8.2.20 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	0	0	0	0	0	0	1	1	06h
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st & 2nd & 3rd Parameter:

Bit	Description
7-0	CHIP_REV

Restriction	

8.2.21 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

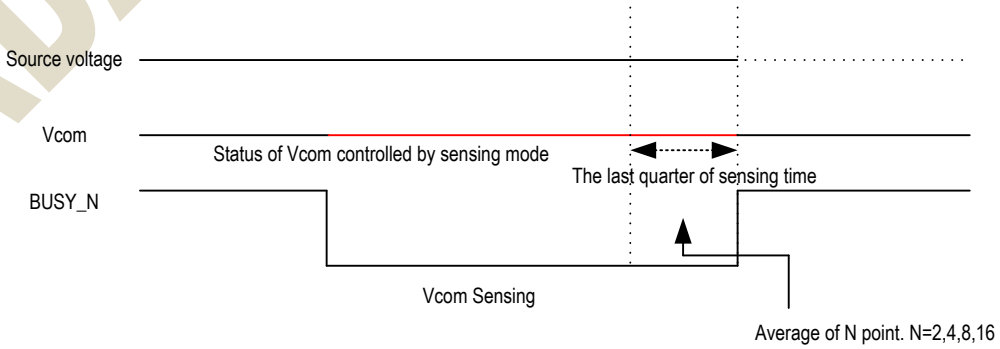
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s
7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16



Restriction: This command only actives when BUSY_N = "1".

8.2.22 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
6-0	VV[6:0]	**VCOM value**

VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

8.2.23 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.
1st Parameter:

Bit	Name	Description
6-0	VDCS[6:0]	**VCOM value**

VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

8.2.24 R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	PTH_ENB	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode
PTH_ENB	0:Source output enable follow HRST and HRED 1:Source output disable

Note:
No matter HRST[1:0] ,HRST[9],HRED[9],VRST[9],VRED[9] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

Gates scan both inside and outside of the partial window.

Restriction

8.2.25 R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

8.2.26 R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.27 R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the MTP								-

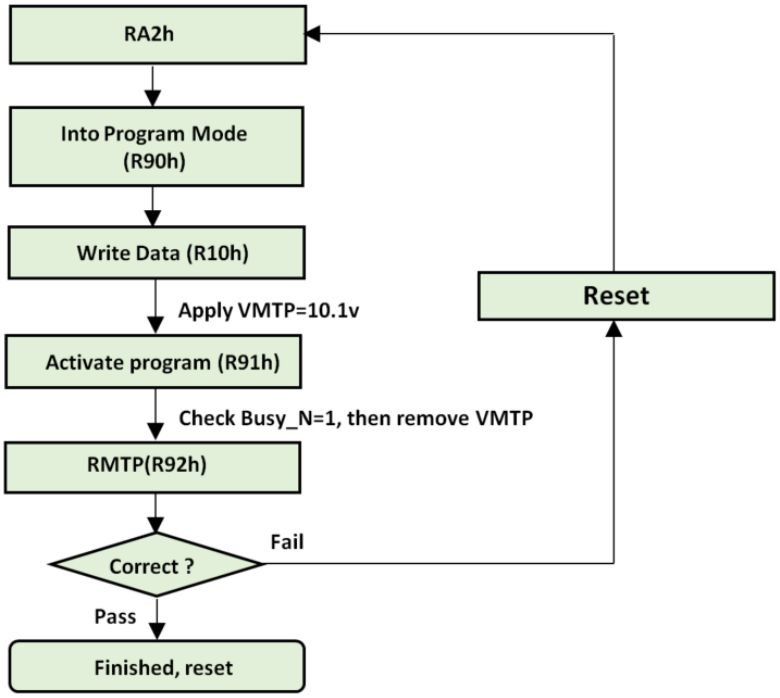
NOTE: "-" Don't care, can be set to VDD or GND level

Description

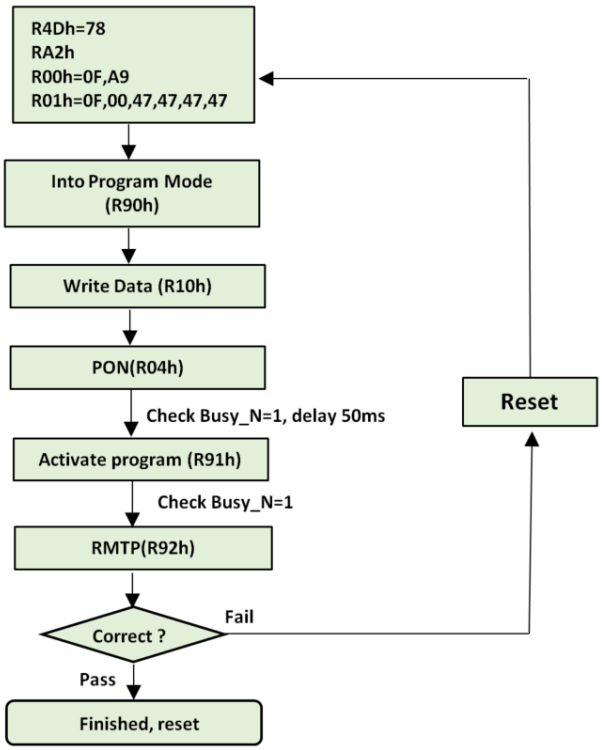
The command define as follows:

-The command is used for reading the content of MTP for checking the data of programming,

-The value of (n) is depending on the amount of programmed data, the max address= 0xFFF



The sequence of programming MTP(External power)



The sequence of programming MTP(Internal power)

Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.28 RA2 (PGM_CFG): MTP Program Config Register

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM_CFG	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
2nd Parameter	W	1	PGM_SADDR[15:8]								00h
3rd Parameter	W	1	PGM_SADDR[7:0]								00h
4th Parameter	W	1	PGM_DSIZE[15:8]								0Fh
5th Parameter	W	1	PGM_DSIZE[7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for setting configuration of MTP

1st Parameter:

Bit	Name	Description
0	S_dis	0: slave enable some command (default) 1: slave disable some command
1	M_dis	0: master enable some command (default) 1: master disable some command
4	VMTPSEL	0:External VMTP (default) 1:Internal VMTP

Bit[0] enable/disable some command when IC sets slave (MS pin is low)
Bit[1] enable/disable some command when IC sets master (MS pin is high)

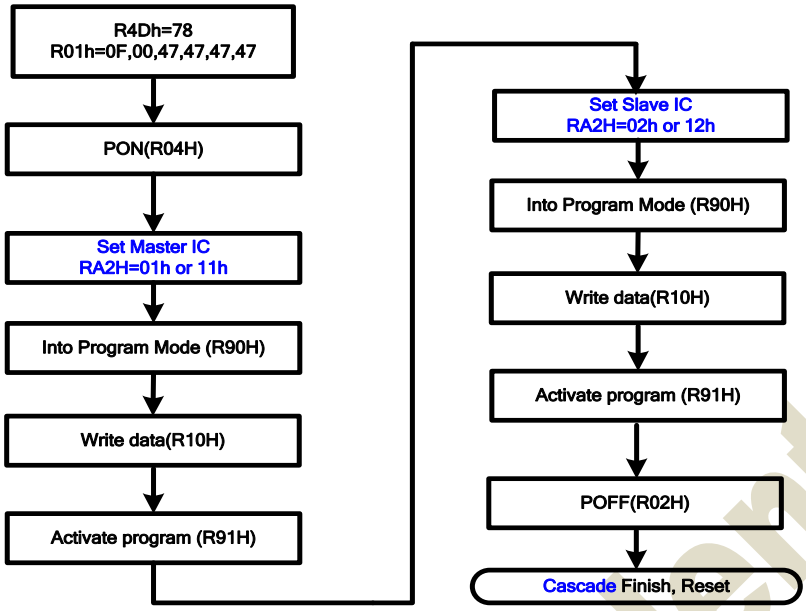
Note:
Some command define: R00H(Parameter 1) (PSR), R10H(DTM), R90H(PGM), R91H(APG), R83H(PTLW)

Command read

M_dis	S_dis	Description
0	0	command read from master
0	1	command read from master
1	0	command read from slave
1	1	command read from slave

2nd & 3rd Parameters: Program and Read MTP start address PGM_SADDR[15:0]
4th & 5th Parameters: Program data size PGM_DSIZE[15:0]

Note:
If user program Area0 (0x00~0x017F), PGM_SADDR[15:0] will be set 0x0000, PGM_DSIZE[15:0] will be set 0x0180.

	Cascade MTP Flow 
Restriction	

8.2.29 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	-	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter:

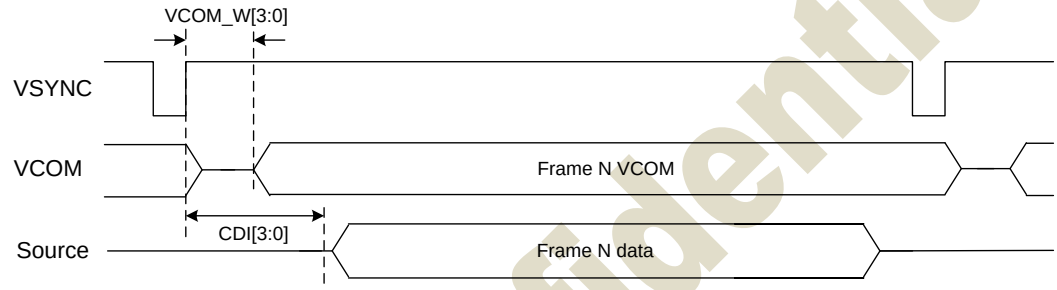
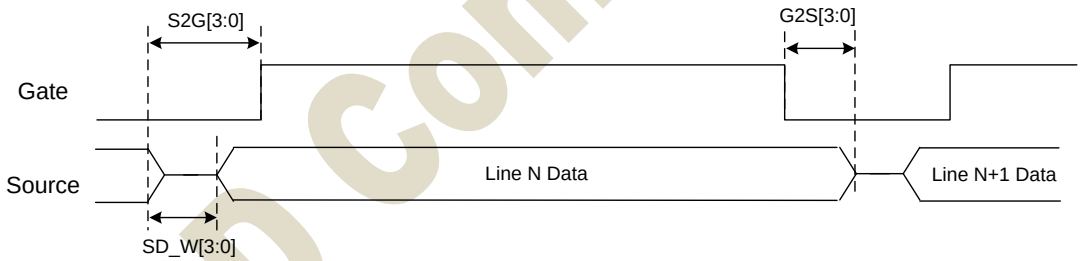
Bit	Name	Description
0	CCEIN	Output clock enable/disable. 0: Output 0V at SyncC pin. (default) 1: Output clock at SyncC pin for slave chip.

Restriction	

8.2.30 RE3H (PWS): Power Saving Register

RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. VCOM_W: VCOM power saving width (unit = line period)  SD_W: Source power saving width (unit = 500nS), SD_W<=S2G 
Restriction	

8.2.31 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection
Restriction	

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

Register Restriction

Following table will indicate the register restriction:

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R04H(PON)	X	Flag
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R17H(AUTO)	Valid in standby	Flag
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R61H(TRES)	X	No action
R65H(GSST)	X	No action
R70H(REV)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R83H(PTL)	X	No action
R90H(PGM)	X	No action
R91H(APG)	X	Flag
R92H(RMTP)	X	Flag
RA2H(PGM_CFG)	X	No action
RE0H(CCSET)	X	No action
RE3H(PWS)	X	No action
RE4H(LVSEL)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

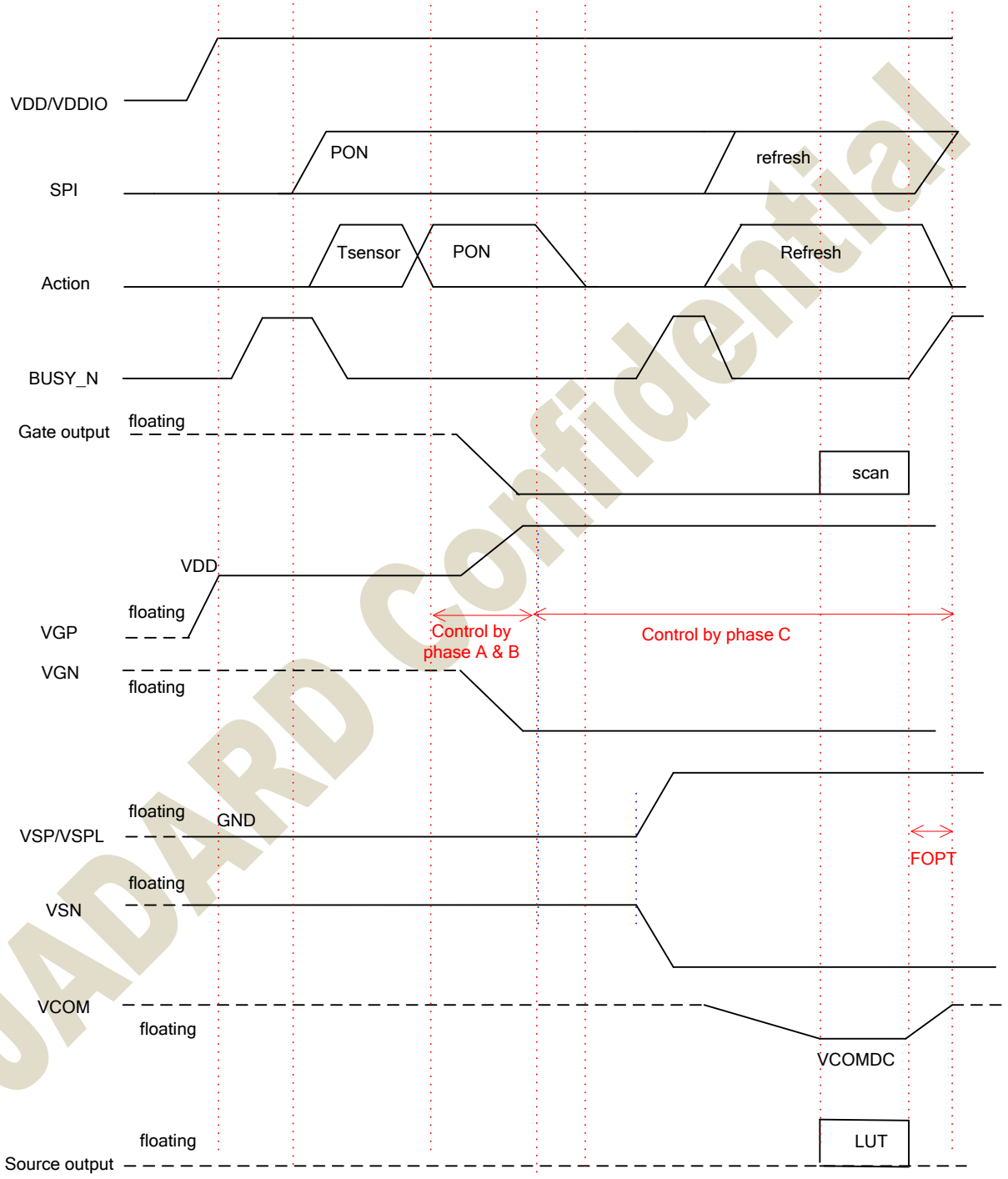


Figure 1: Power on sequence

Power off Sequence

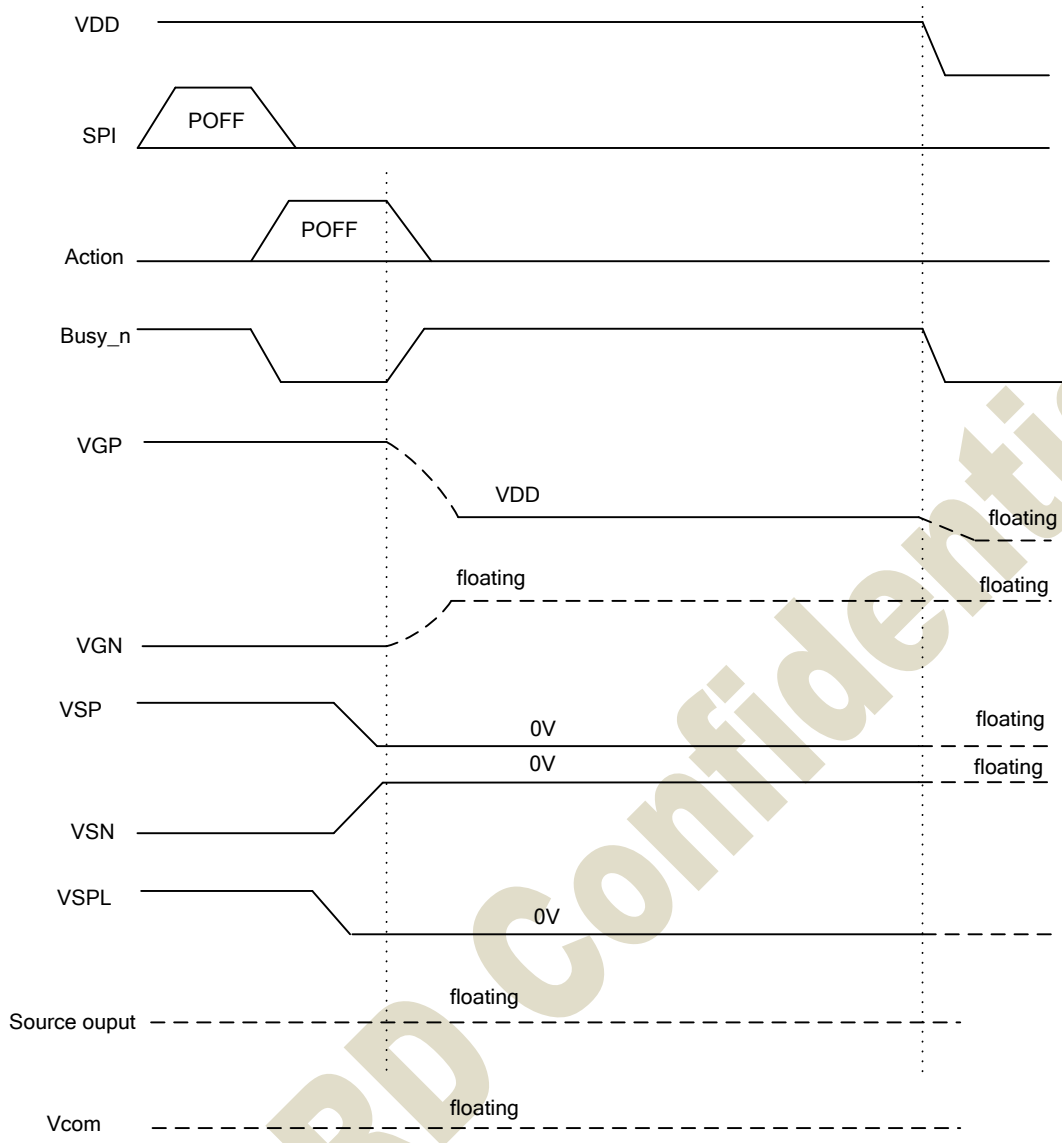


Figure 2: Power off sequence

DSLP sequence

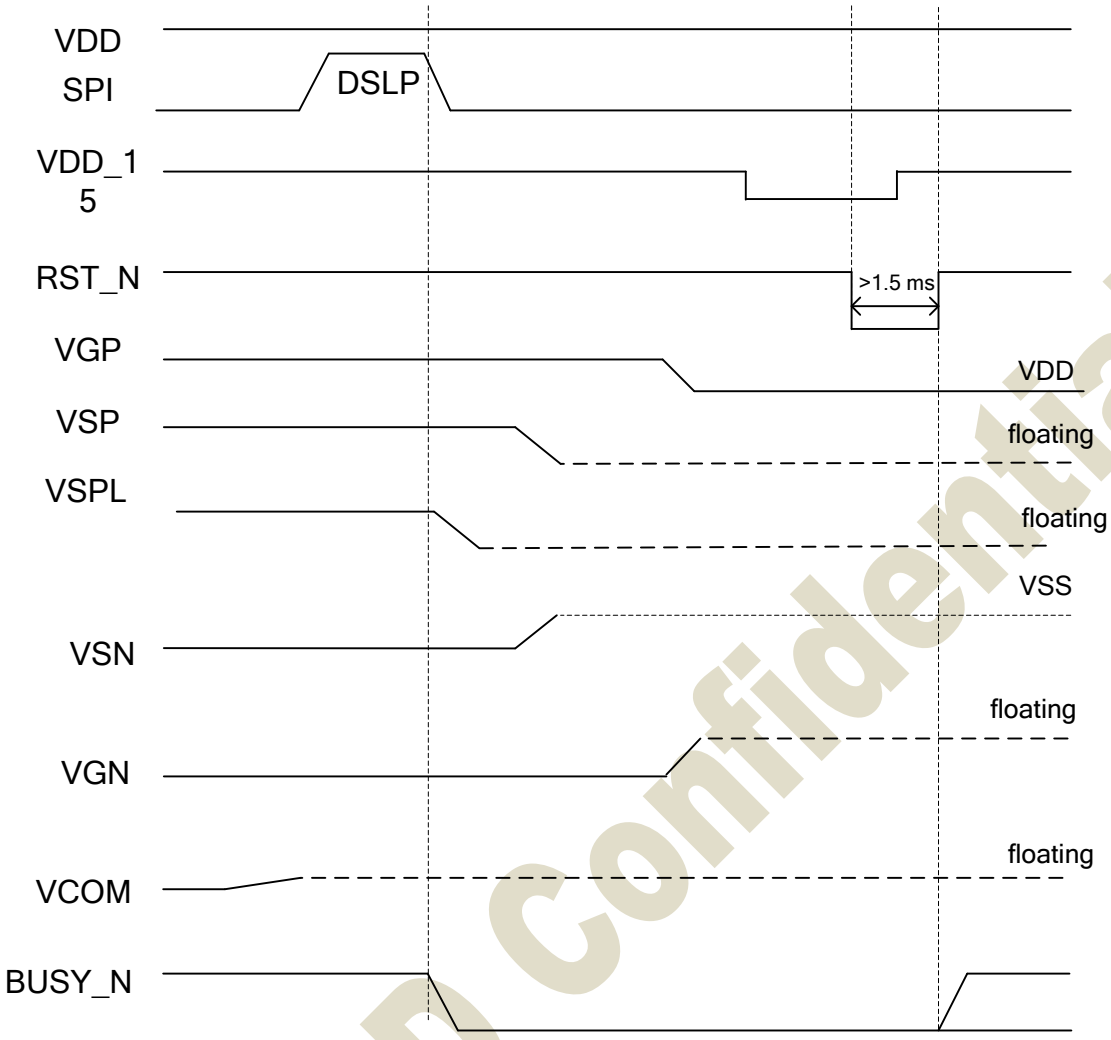


Figure 4: DSLP sequence

9.2 MTP LUT Definition

The MTP size would be 4096 Bytes.

MTP bank 0 (4K bytes)	
Address(Hex)	Content
0x000~0xEFF	LUT Compress data
0xF00~0xF58	Reserved
0xF59~0xF84	Default setting
0xF85~0xFFF	JD setting

9.3 Default Setting Format in MTP

	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
			User Reserved bytes								FF
--	3929	F59	Enable MTP Setting (0xA5)								A5
-	3930	F5A	Reserved								-
	3931	F5B	Reserved								-
R00H	3932	F5C	RES[1:0]		PST_MODE	-	UD	SHL	SHD_N	RST_N	0F
	3933	F5D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09
R01H	3934	F5E	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07
	3935	F5F	-	-	-		-	-	VGP[1:0]		00
	3936	F60	-	VSPL_0[6:0]							00
	3937	F61	-	VSP_1[6:0]							00
	3938	F62	-	VSN_1[6:0]							00
	3939	F63	-	VSPL_1[6:0]							00
-	3940	F64	Reserved								00
	3941	F65	Reserved								00
	3942	F66	Reserved								54
	3943	F67	Reserved								44
R06H	3944	F68	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00
	3945	F69	-	-	PHA_ON[5:0]						06
	3946	F6A	-	-	PHA_OFF[5:0]						02
	3947	F6B	-	-	PHB_ON[5:0]						07
	3948	F6C	-	-	PHB_OFF[5:0]						02
	3949	F6D	-	-	PHC_ON[5:0]						07
	3950	F6E	-	-	PHC_OFF[5:0]						02
-	3951	F6F	Reserved								00
R30H	3952	F70	-	-	-	-	Dyna	FR[2:0]			02
R50h	3953	F71	VBD[2:0]			DDX	CDI[3:0]				97
-	3954	F72	Reserved								02
	3955	F73	Reserved								02
R61H	3956	F74	-	-	-	-	-	-	HRES[9]	HRES[8]	00
	3957	F75	HRES[7:2]						0	0	00
	3958	F76	-	-	-	-	-	-	VRES[9]	VRES[8]	00
	3959	F77	VRES[7:0]								00
R65H	3960	F78	-	-	-	-	-	-	S_start(9)	S_start(8)	00
	3961	F79	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00
	3962	F7A	-	-	-	-	-	-	G_start(9)	G_start(8)	00
	3963	F7B	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00
R82H	3964	F7C		VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00
-	3965	F7D	Reserved								00
R41H	3966	F7E	-	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00
	3967	F7F	Reserved								00
RE3H	3968	F80	VCOM_W[3:0]				SD_W[3:0]				00
RE4H	3969	F81	-	-	-	-	-	-	LVD_SEL[1:0]		03
-	3970	F82	Reserved								03
	3971	F83	Reserved								1C
	3972	F84	Reserved								00
--	3973-4095	F85-FFF	JD setting								FF

9.4 Data transmission waveform

Example1: The driver will scan 1 frame to GND after waveform finished.(FOPT=0)

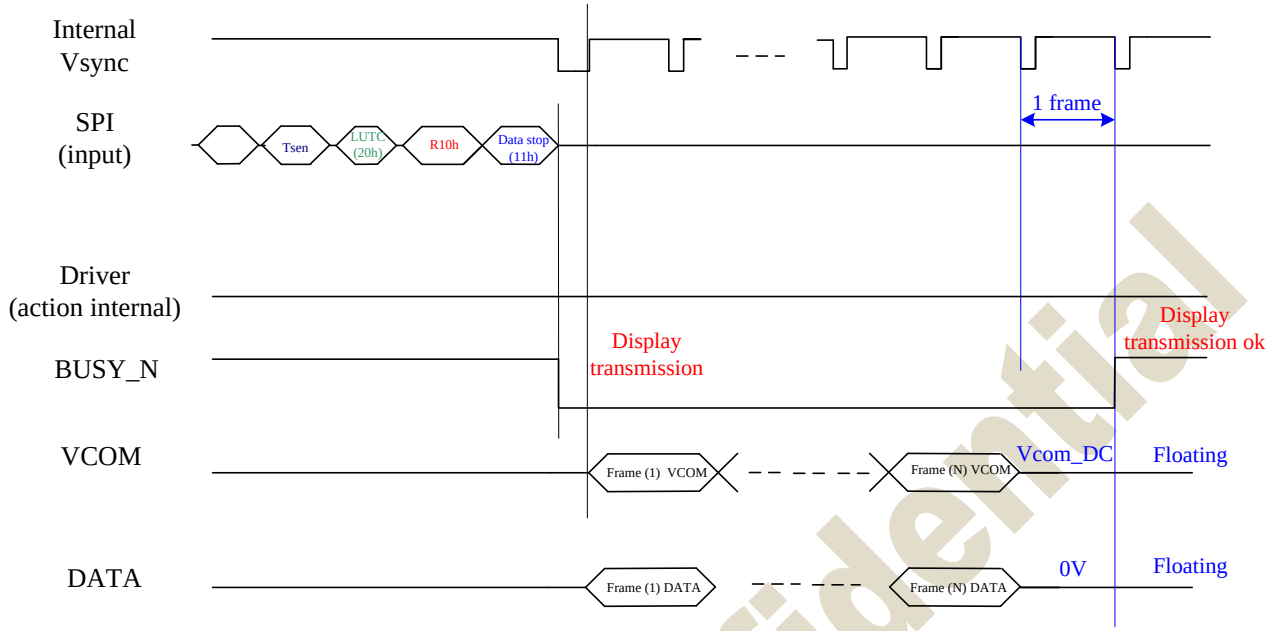


Figure 1: Data transmission example1 waveform

Example2: The driver will float VCOM and keep previous output data(FOPT=1)

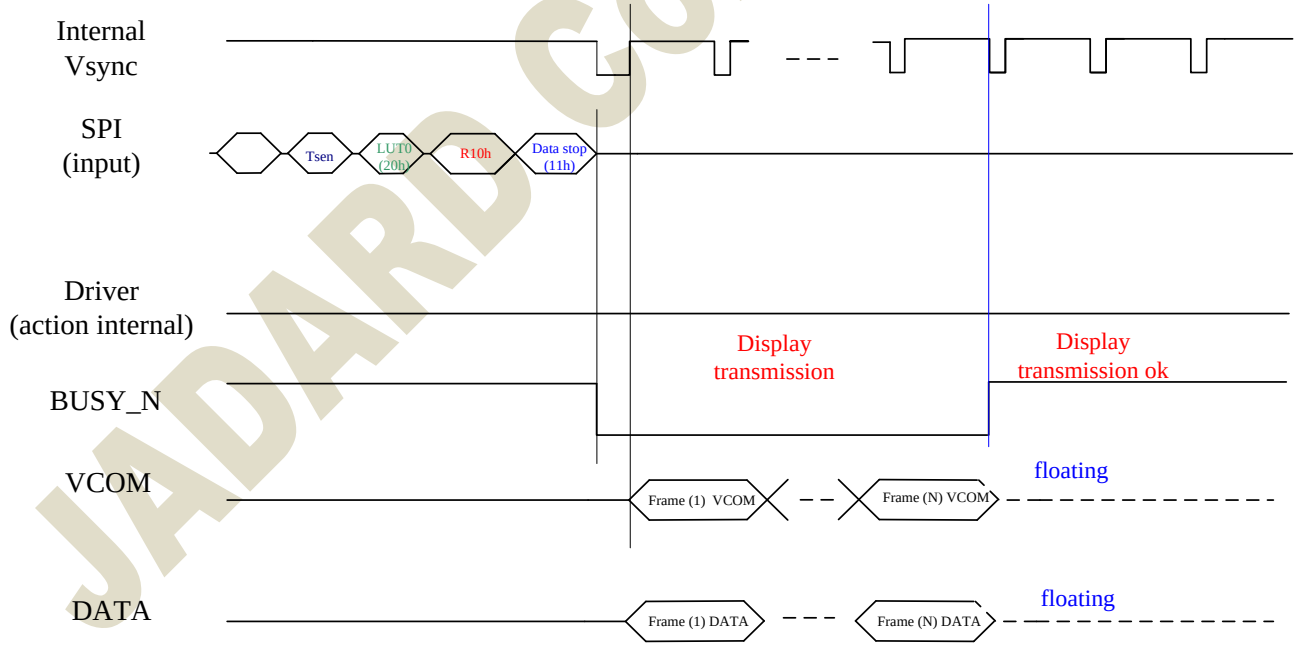


Figure 2: Display refresh example2 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGP-VGN	VGN-0.3	VGP+0.3	V
Analog supply	VSP_0	+15	+15	V
Analog supply	VSN_0	-15	-15	V
Analog supply	VSPL_0	+3	+15	V
Analog supply	VSP_1	+3	+15	V
Analog supply	VSN_1	-3	-15	V
Analog supply	VSPL_1	+3	+15	V
Supply voltage	VGP	+10	+20	V
Supply voltage	VGN	-20	-10	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.5V output voltage	VDD_15	1.35	1.5	1.65		
1.5V input voltage	VDD_15	1.35	1.5	1.65		
MTP program power	VMTP	9.8	10.1	10.2		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3Xvdd	V	Digital input pins
High Level Input Voltage	Vih	0.7Xvio	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400Ma
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400Ma DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400Ma
Input Leakage Current	Iin	-1.0	-	+1.0	Ua	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	Ua	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	Ma	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	Ua	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	Ma	No load
Operating Current	IVDD1*	-	-	TBD	Ma	
Operating temperature	T_{op}	-30	-	85	℃	

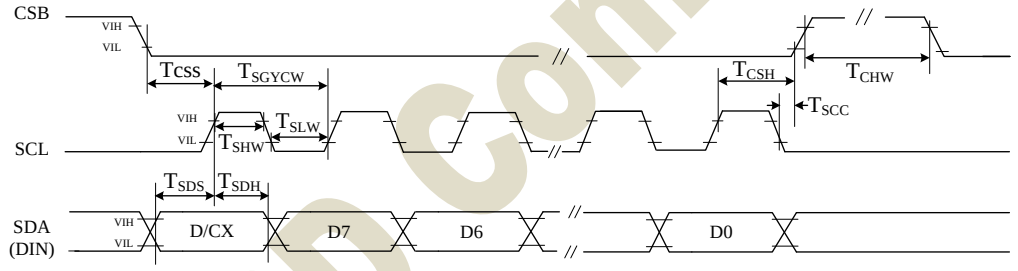
NOTE: typ. And max. values to be confirmed by design

10.3 Analog DC Characteristics

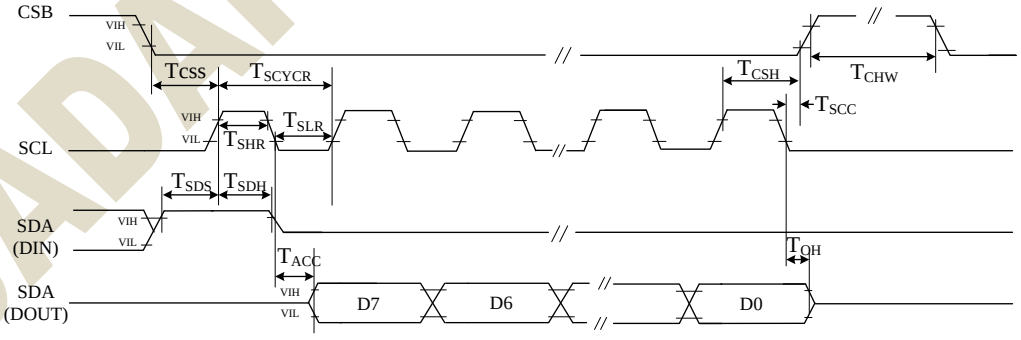
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSP	-	15	-	V	For source driver/VCOM
Positive Source voltage dev	Dvsp	-100	0	+100	Mv	
Negative Source voltage	VSn	-	-15	-	V	For source driver/VCOM
Negative Source voltage dev	Dvsn	-100	-	+100	Mv	
Positive Source voltage	VSPL_0	3		15		
Positive Source voltage dev.	Dvspl_0	-100	-	+100	Mv	
Positive Source voltage	VSP_1	3		15		
Positive Source voltage dev.	Dvsp_1	-100	-	+100	Mv	
Positive Source voltage	VSPL_1	3		15		
Positive Source voltage dev.	Dvspl_1	-100	-	+100	Mv	
VCOM voltage dev.	Dvcom	-200	-	+200	Mv	
Positive gate voltage dev	Dvgp	-500	-	+500	Mv	
Dynamic Range of Output	Vdr	0.1	-	VSP-0.1	V	
Voltage Range of VGP – VGN	VGP-VGN	-	-	41	V	
Negative Gate voltage	VGN	-10	-	-20	V	For gate driver
Positive Gate voltage	VGP	10		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGP*	-	0	0.2	Ua	Include VSP power With load
Positive HV Operating Current	IVGP*	-	0.7	1.1	Ma	Include VSP power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGP*	-	0.8	1.2	Ma	Include VSP power With load all SD=H VCOM external resistor divider not Included
Negative HV Stand-by Current (power off mode)	IstVGN*	-	0	0.2	Ma	Include VSP power With load
Negative HV Operating Current	IVGN*	-	0.8	1.2	Ma	Include VSN power With load all SD=L
Negative HV Operating Current	IVGN*	-	0.9-	1.3	Ma	Include VSN power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*	-	0	0.01	Ma	
VINT1 Operating Current	IVINT1*	-	-	0.3	Ma	
Voltage	IVINT1*	-	-	0.3	Ma	

10.4 AC Characteristics

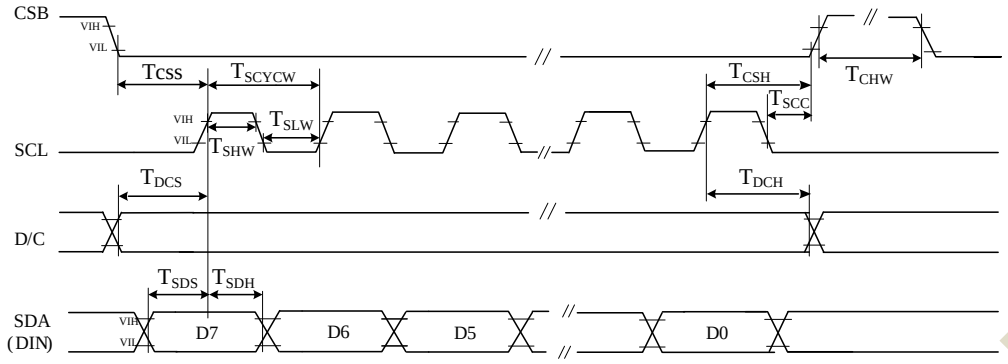
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	250			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time



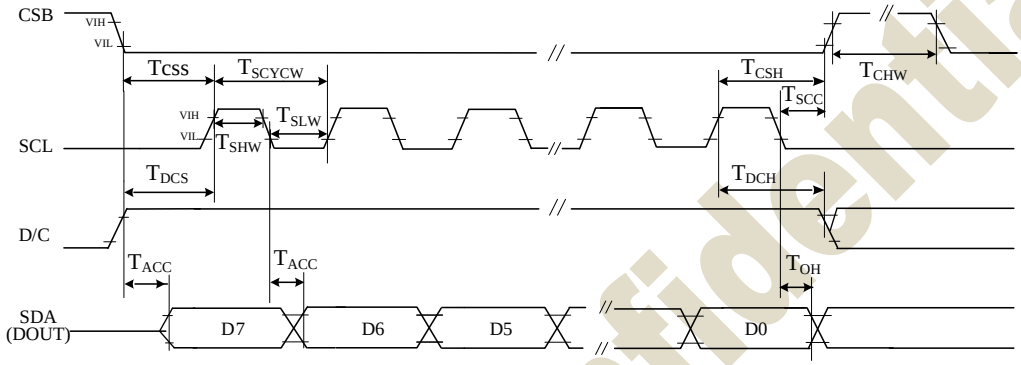
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

Figure 9: SPI interface timing

11. CHIP OUTLINE DIMENSIONS

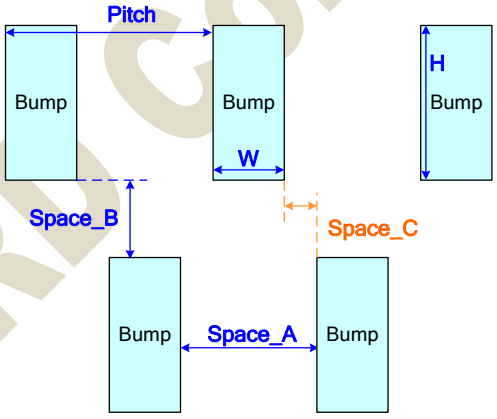
11.1 Circuit/Bump View

G1 G3 G5 ... S399 ~ S0 ... G4 G2 G0

JD79668
(face up)

Die Size:	**13019um * 725um**
Die Thickness:	230 μm ± 20μm (Polish)
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μm
Bump Height:	9 μm ± 2μm
	(H_{MAX} – H_{MIN}) within die ⩽ 2μm
Hardness:	75 Hv ±25Hv
Coordinate origin:	Chip center

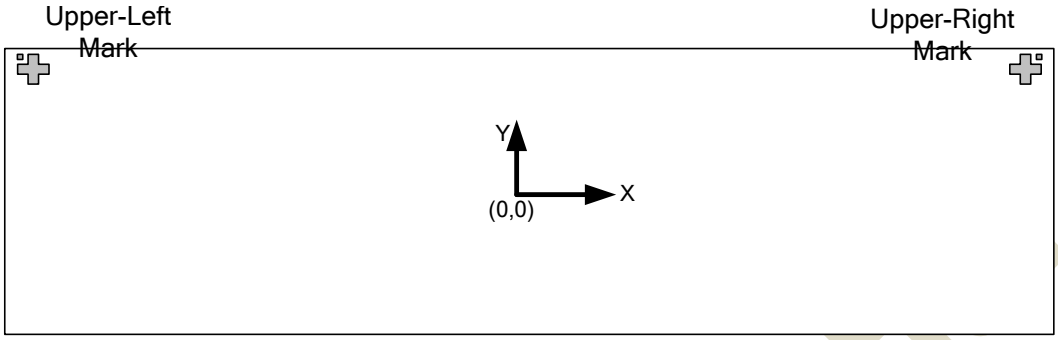
11.2 Bump information



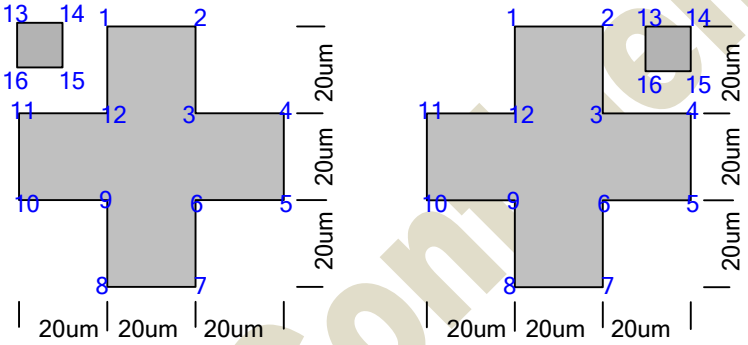
Bump type	Pitch	Space_A	Space_B	Space_C	W	H	area(um2)	Q'ty	Total area(um2)
Input PAD	46	18	-	-	28	60	1680	281	472080
Source PAD	28	12	25	(-2)	16	65	1040	406	422240
Gate PAD	42	25	25	4	17	60	1020	326	332520
							Total	1013	1226840

12. ALIGNMENT MARK INFORMATION

12.1 Location



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-6465.0	300.5	6465.0	300.5
1	-6475.0	330.5	6455.0	330.5
2	-6455.0	330.5	6475.0	330.5
3	-6455.0	310.5	6475.0	310.5
4	-6435.0	310.5	6495.0	310.5
5	-6435.0	290.5	6495.0	290.5
6	-6455.0	290.5	6475.0	290.5
7	-6455.0	270.5	6475.0	270.5
8	-6475.0	270.5	6455.0	270.5
9	-6475.0	290.5	6455.0	290.5
10	-6495.0	290.5	6435.0	290.5
11	-6495.0	310.5	6435.0	310.5
12	-6475.0	310.5	6455.0	310.5
13	-6495.0	330.5	6485.0	330.5
14	-6485.0	330.5	6495.0	330.5
15	-6485.0	320.5	6495.0	320.5
16	-6495.0	320.5	6485.0	320.5

12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	T_N18V	-6440	-321.5	28	60
2	VCOM	-6394	-321.5	28	60
3	VCOM	-6348	-321.5	28	60
4	VCOM	-6302	-321.5	28	60
5	VCOM	-6256	-321.5	28	60
6	VCOM	-6210	-321.5	28	60
7	VCOM	-6164	-321.5	28	60
8	VCOM	-6118	-321.5	28	60
9	VCOM	-6072	-321.5	28	60
10	VSSA	-6026	-321.5	28	60
11	VGN	-5980	-321.5	28	60
12	VGN	-5934	-321.5	28	60
13	VGN	-5888	-321.5	28	60
14	VGN	-5842	-321.5	28	60
15	VGN	-5796	-321.5	28	60
16	VGN	-5750	-321.5	28	60
17	VGN	-5704	-321.5	28	60
18	VGN	-5658	-321.5	28	60
19	VGN	-5612	-321.5	28	60
20	VGN	-5566	-321.5	28	60
21	VGN	-5520	-321.5	28	60
22	VGN	-5474	-321.5	28	60
23	VGN	-5428	-321.5	28	60
24	VGN	-5382	-321.5	28	60
25	VGN	-5336	-321.5	28	60
26	VGN	-5290	-321.5	28	60
27	VSSA	-5244	-321.5	28	60
28	VSN	-5198	-321.5	28	60
29	VSN	-5152	-321.5	28	60
30	VSN	-5106	-321.5	28	60
31	VSN	-5060	-321.5	28	60
32	VSN	-5014	-321.5	28	60
33	VSN	-4968	-321.5	28	60
34	VSN	-4922	-321.5	28	60
35	VSN	-4876	-321.5	28	60
36	VSN	-4830	-321.5	28	60
37	VSN	-4784	-321.5	28	60
38	VSSA	-4738	-321.5	28	60
39	VGP	-4692	-321.5	28	60
40	VGP	-4646	-321.5	28	60
41	VGP	-4600	-321.5	28	60
42	VGP	-4554	-321.5	28	60
43	VGP	-4508	-321.5	28	60
44	VGP	-4462	-321.5	28	60
45	VGP	-4416	-321.5	28	60
46	VGP	-4370	-321.5	28	60
47	VGP	-4324	-321.5	28	60
48	VGP	-4278	-321.5	28	60
49	VGP	-4232	-321.5	28	60
50	VGP	-4186	-321.5	28	60
51	VGP	-4140	-321.5	28	60
52	VGP	-4094	-321.5	28	60
53	VSSA	-4048	-321.5	28	60
54	VSP	-4002	-321.5	28	60
55	VSP	-3956	-321.5	28	60
56	VSP	-3910	-321.5	28	60
57	VSP	-3864	-321.5	28	60
58	VSP	-3818	-321.5	28	60

No.	Name	X-axis	Y-axis	W	H
59	VSP	-3772	-321.5	28	60
60	VSP	-3726	-321.5	28	60
61	VSP	-3680	-321.5	28	60
62	VSP	-3634	-321.5	28	60
63	VSP	-3588	-321.5	28	60
64	VSSA	-3542	-321.5	28	60
65	VMTP	-3496	-321.5	28	60
66	VMTP	-3450	-321.5	28	60
67	VMTP	-3404	-321.5	28	60
68	VMTP	-3358	-321.5	28	60
69	VMTP	-3312	-321.5	28	60
70	VMTP	-3266	-321.5	28	60
71	VMTP	-3220	-321.5	28	60
72	VDD_15V	-3174	-321.5	28	60
73	VDD_15V	-3128	-321.5	28	60
74	VDD_15V	-3082	-321.5	28	60
75	VDD_15V	-3036	-321.5	28	60
76	VDD_15V	-2990	-321.5	28	60
77	VDD_15V	-2944	-321.5	28	60
78	VDD_15V	-2898	-321.5	28	60
79	VDD_15V	-2852	-321.5	28	60
80	VDD_15V	-2806	-321.5	28	60
81	VDD_15V	-2760	-321.5	28	60
82	VSSA	-2714	-321.5	28	60
83	VSSA	-2668	-321.5	28	60
84	VSSA	-2622	-321.5	28	60
85	VSSA	-2576	-321.5	28	60
86	VSSA	-2530	-321.5	28	60
87	VSSA	-2484	-321.5	28	60
88	VSSA	-2438	-321.5	28	60
89	VSSA	-2392	-321.5	28	60
90	VSSA	-2346	-321.5	28	60
91	VSSA	-2300	-321.5	28	60
92	VSSA	-2254	-321.5	28	60
93	VSSA	-2208	-321.5	28	60
94	VSS	-2162	-321.5	28	60
95	VSS	-2116	-321.5	28	60
96	VSS	-2070	-321.5	28	60
97	VSS	-2024	-321.5	28	60
98	VSS	-1978	-321.5	28	60
99	VSS	-1932	-321.5	28	60
100	VSS	-1886	-321.5	28	60
101	VSS	-1840	-321.5	28	60
102	VSS	-1794	-321.5	28	60
103	VSS	-1748	-321.5	28	60
104	VSS	-1702	-321.5	28	60
105	VSS	-1656	-321.5	28	60
106	VDD	-1610	-321.5	28	60
107	VDD	-1564	-321.5	28	60
108	VDD	-1518	-321.5	28	60
109	VDD	-1472	-321.5	28	60
110	VDD	-1426	-321.5	28	60
111	VDD	-1380	-321.5	28	60
112	VDD	-1334	-321.5	28	60
113	VDD	-1288	-321.5	28	60
114	VDD	-1242	-321.5	28	60
115	VDD	-1196	-321.5	28	60
116	VDDP	-1150	-321.5	28	60

No.	Name	X-axis	Y-axis	W	H
117	VDDP	-1104	-321.5	28	60
118	VDDP	-1058	-321.5	28	60
119	VDDP	-1012	-321.5	28	60
120	VDDP	-966	-321.5	28	60
121	VDDP	-920	-321.5	28	60
122	VDDP	-874	-321.5	28	60
123	T_LDON5V	-828	-321.5	28	60
124	DUMMY[0]	-782	-321.5	28	60
125	T_VTSEN	-736	-321.5	28	60
126	T_SAR_REF	-690	-321.5	28	60
127	T_VREF	-644	-321.5	28	60
128	T_EN_LSH	-598	-321.5	28	60
129	T_IBIAS	-552	-321.5	28	60
130	T_VSPD_REF	-506	-321.5	28	60
131	T_VCOM	-460	-321.5	28	60
132	T_IN[2]	-414	-321.5	28	60
133	DUMMY[1]	-368	-321.5	28	60
134	T_IN[1]	-322	-321.5	28	60
135	DUMMY[2]	-276	-321.5	28	60
136	T_IN[0]	-230	-321.5	28	60
137	DUMMY[3]	-184	-321.5	28	60
138	T_DEBUG[8]	-138	-321.5	28	60
139	DUMMY[4]	-92	-321.5	28	60
140	T_DEBUG[7]	-46	-321.5	28	60
141	DUMMY[5]	0	-321.5	28	60
142	T_DEBUG[6]	46	-321.5	28	60
143	DUMMY[6]	92	-321.5	28	60
144	T_DEBUG[5]	138	-321.5	28	60
145	DUMMY[7]	184	-321.5	28	60
146	T_DEBUG[4]	230	-321.5	28	60
147	DUMMY[8]	276	-321.5	28	60
148	T_DEBUG[3]	322	-321.5	28	60
149	DUMMY[9]	368	-321.5	28	60
150	T_DEBUG[2]	414	-321.5	28	60
151	DUMMY[10]	460	-321.5	28	60
152	T_DEBUG[1]	506	-321.5	28	60
153	DUMMY[11]	552	-321.5	28	60
154	T_DEBUG[0]	598	-321.5	28	60
155	DUMMY[12]	644	-321.5	28	60
156	T_EX_SYSCLK	690	-321.5	28	60
157	DUMMY[13]	736	-321.5	28	60
158	T_EX_REFCLK	782	-321.5	28	60
159	DUMMY[14]	828	-321.5	28	60
160	DUMMY[15]	874	-321.5	28	60
161	VSS	920	-321.5	28	60
162	DUMMY[16]	966	-321.5	28	60
163	T_EN_DIG	1012	-321.5	28	60
164	DUMMY[17]	1058	-321.5	28	60
165	VDDIO	1104	-321.5	28	60
166	VDDIO	1150	-321.5	28	60
167	VDDIO	1196	-321.5	28	60
168	VDDIO	1242	-321.5	28	60
169	DUMMY[18]	1288	-321.5	28	60
170	DUMMY[19]	1334	-321.5	28	60
171	DUMMY[20]	1380	-321.5	28	60
172	DUMMY[21]	1426	-321.5	28	60
173	DUMMY[22]	1472	-321.5	28	60
174	DUMMY[23]	1518	-321.5	28	60
175	DUMMY[24]	1564	-321.5	28	60
176	SDA	1610	-321.5	28	60

No.	Name	X-axis	Y-axis	W	H
177	SCL	1656	-321.5	28	60
178	VSS	1702	-321.5	28	60
179	CSB	1748	-321.5	28	60
180	VDDIO	1794	-321.5	28	60
181	DUMMY[25]	1840	-321.5	28	60
182	DUMMY[26]	1886	-321.5	28	60
183	VSS	1932	-321.5	28	60
184	DC	1978	-321.5	28	60
185	VDDIO	2024	-321.5	28	60
186	DUMMY[27]	2070	-321.5	28	60
187	DUMMY[28]	2116	-321.5	28	60
188	DUMMY[29]	2162	-321.5	28	60
189	DUMMY[30]	2208	-321.5	28	60
190	RST_N	2254	-321.5	28	60
191	BUSY_N	2300	-321.5	28	60
192	VSS	2346	-321.5	28	60
193	DUMMY[31]	2392	-321.5	28	60
194	DUMMY[32]	2438	-321.5	28	60
195	DUMMY[33]	2484	-321.5	28	60
196	SYNCD	2530	-321.5	28	60
197	SYNCE	2576	-321.5	28	60
198	SYNCC	2622	-321.5	28	60
199	SYNCE	2668	-321.5	28	60
200	SYNCD	2714	-321.5	28	60
201	DUMMY[34]	2760	-321.5	28	60
202	VDDIO	2806	-321.5	28	60
203	DUMMY[35]	2852	-321.5	28	60
204	VSS	2898	-321.5	28	60
205	DUMMY[36]	2944	-321.5	28	60
206	VDDIO	2990	-321.5	28	60
207	BS	3036	-321.5	28	60
208	VSS	3082	-321.5	28	60
209	DUMMY[37]	3128	-321.5	28	60
210	VDDIO	3174	-321.5	28	60
211	PCKI	3220	-321.5	28	60
212	VSS	3266	-321.5	28	60
213	MS	3312	-321.5	28	60
214	VDDIO	3358	-321.5	28	60
215	VSS	3404	-321.5	28	60
216	TSDA	3450	-321.5	28	60
217	TSDA	3496	-321.5	28	60
218	TSCL	3542	-321.5	28	60
219	TSCL	3588	-321.5	28	60
220	VSS	3634	-321.5	28	60
221	PCKO	3680	-321.5	28	60
222	DUMMY[38]	3726	-321.5	28	60
223	VSS	3772	-321.5	28	60
224	DUMMY[39]	3818	-321.5	28	60
225	DUMMY[40]	3864	-321.5	28	60
226	VSS	3910	-321.5	28	60
227	DUMMY[41]	3956	-321.5	28	60
228	DUMMY[42]	4002	-321.5	28	60
229	VSS	4048	-321.5	28	60
230	DUMMY[43]	4094	-321.5	28	60
231	DUMMY[44]	4140	-321.5	28	60
232	VSS	4186	-321.5	28	60
233	DUMMY[45]	4232	-321.5	28	60
234	DUMMY[46]	4278	-321.5	28	60
235	DUMMY[47]	4324	-321.5	28	60
236	DUMMY[48]	4370	-321.5	28	60

No.	Name	X-axis	Y-axis	W	H
237	DUMMY[49]	4416	-321.5	28	60
238	DUMMY[50]	4462	-321.5	28	60
239	DUMMY[51]	4508	-321.5	28	60
240	DUMMY[52]	4554	-321.5	28	60
241	DUMMY[53]	4600	-321.5	28	60
242	DUMMY[54]	4646	-321.5	28	60
243	VSPL	4692	-321.5	28	60
244	VSPL	4738	-321.5	28	60
245	VSPL	4784	-321.5	28	60
246	VSPL	4830	-321.5	28	60
247	VSPL	4876	-321.5	28	60
248	VSPL	4922	-321.5	28	60
249	VSPL	4968	-321.5	28	60
250	VSPL	5014	-321.5	28	60
251	DUMMY[55]	5060	-321.5	28	60
252	DUMMY[56]	5106	-321.5	28	60
253	DUMMY[57]	5152	-321.5	28	60
254	DUMMY[58]	5198	-321.5	28	60
255	DUMMY[59]	5244	-321.5	28	60
256	DUMMY[60]	5290	-321.5	28	60
257	VSS	5336	-321.5	28	60
258	FB	5382	-321.5	28	60
259	FB	5428	-321.5	28	60
260	VSS	5474	-321.5	28	60
261	RESE	5520	-321.5	28	60
262	RESE	5566	-321.5	28	60
263	VSS	5612	-321.5	28	60
264	GDR	5658	-321.5	28	60
265	GDR	5704	-321.5	28	60
266	GDR	5750	-321.5	28	60
267	GDR	5796	-321.5	28	60
268	GDR	5842	-321.5	28	60
269	GDR	5888	-321.5	28	60
270	GDR	5934	-321.5	28	60
271	GDR	5980	-321.5	28	60
272	VSS	6026	-321.5	28	60
273	VCOM	6072	-321.5	28	60
274	VCOM	6118	-321.5	28	60
275	VCOM	6164	-321.5	28	60
276	VCOM	6210	-321.5	28	60
277	VCOM	6256	-321.5	28	60
278	VCOM	6302	-321.5	28	60
279	VCOM	6348	-321.5	28	60
280	VCOM	6394	-321.5	28	60
281	DUMMY[61]	6440	-321.5	28	60
282	DUMMY[62]	6345	231.5	17	60
283	DUMMY[63]	6324	316.5	17	60
284	DUMMY[64]	6303	231.5	17	60
285	DUMMY[65]	6282	316.5	17	60
286	DUMMY[66]	6261	231.5	17	60
287	DUMMY[67]	6240	316.5	17	60
288	G[0]	6219	231.5	17	60
289	G[2]	6198	316.5	17	60
290	G[4]	6177	231.5	17	60
291	G[6]	6156	316.5	17	60
292	G[8]	6135	231.5	17	60
293	G[10]	6114	316.5	17	60
294	G[12]	6093	231.5	17	60
295	G[14]	6072	316.5	17	60
296	G[16]	6051	231.5	17	60

No.	Name	X-axis	Y-axis	W	H
297	G[18]	6030	316.5	17	60
298	G[20]	6009	231.5	17	60
299	G[22]	5988	316.5	17	60
300	G[24]	5967	231.5	17	60
301	G[26]	5946	316.5	17	60
302	G[28]	5925	231.5	17	60
303	G[30]	5904	316.5	17	60
304	G[32]	5883	231.5	17	60
305	G[34]	5862	316.5	17	60
306	G[36]	5841	231.5	17	60
307	G[38]	5820	316.5	17	60
308	G[40]	5799	231.5	17	60
309	G[42]	5778	316.5	17	60
310	G[44]	5757	231.5	17	60
311	G[46]	5736	316.5	17	60
312	G[48]	5715	231.5	17	60
313	G[50]	5694	316.5	17	60
314	G[52]	5673	231.5	17	60
315	G[54]	5652	316.5	17	60
316	G[56]	5631	231.5	17	60
317	G[58]	5610	316.5	17	60
318	G[60]	5589	231.5	17	60
319	G[62]	5568	316.5	17	60
320	G[64]	5547	231.5	17	60
321	G[66]	5526	316.5	17	60
322	G[68]	5505	231.5	17	60
323	G[70]	5484	316.5	17	60
324	G[72]	5463	231.5	17	60
325	G[74]	5442	316.5	17	60
326	G[76]	5421	231.5	17	60
327	G[78]	5400	316.5	17	60
328	G[80]	5379	231.5	17	60
329	G[82]	5358	316.5	17	60
330	G[84]	5337	231.5	17	60
331	G[86]	5316	316.5	17	60
332	G[88]	5295	231.5	17	60
333	G[90]	5274	316.5	17	60
334	G[92]	5253	231.5	17	60
335	G[94]	5232	316.5	17	60
336	G[96]	5211	231.5	17	60
337	G[98]	5190	316.5	17	60
338	G[100]	5169	231.5	17	60
339	G[102]	5148	316.5	17	60
340	G[104]	5127	231.5	17	60
341	G[106]	5106	316.5	17	60
342	G[108]	5085	231.5	17	60
343	G[110]	5064	316.5	17	60
344	G[112]	5043	231.5	17	60
345	G[114]	5022	316.5	17	60
346	G[116]	5001	231.5	17	60
347	G[118]	4980	316.5	17	60
348	G[120]	4959	231.5	17	60
349	G[122]	4938	316.5	17	60
350	G[124]	4917	231.5	17	60
351	G[126]	4896	316.5	17	60
352	G[128]	4875	231.5	17	60
353	G[130]	4854	316.5	17	60
354	G[132]	4833	231.5	17	60
355	G[134]	4812	316.5	17	60
356	G[136]	4791	231.5	17	60

No.	Name	X-axis	Y-axis	W	H
357	G[138]	4770	316.5	17	60
358	G[140]	4749	231.5	17	60
359	G[142]	4728	316.5	17	60
360	G[144]	4707	231.5	17	60
361	G[146]	4686	316.5	17	60
362	G[148]	4665	231.5	17	60
363	G[150]	4644	316.5	17	60
364	G[152]	4623	231.5	17	60
365	G[154]	4602	316.5	17	60
366	G[156]	4581	231.5	17	60
367	G[158]	4560	316.5	17	60
368	G[160]	4539	231.5	17	60
369	G[162]	4518	316.5	17	60
370	G[164]	4497	231.5	17	60
371	G[166]	4476	316.5	17	60
372	G[168]	4455	231.5	17	60
373	G[170]	4434	316.5	17	60
374	G[172]	4413	231.5	17	60
375	G[174]	4392	316.5	17	60
376	G[176]	4371	231.5	17	60
377	G[178]	4350	316.5	17	60
378	G[180]	4329	231.5	17	60
379	G[182]	4308	316.5	17	60
380	G[184]	4287	231.5	17	60
381	G[186]	4266	316.5	17	60
382	G[188]	4245	231.5	17	60
383	G[190]	4224	316.5	17	60
384	G[192]	4203	231.5	17	60
385	G[194]	4182	316.5	17	60
386	G[196]	4161	231.5	17	60
387	G[198]	4140	316.5	17	60
388	G[200]	4119	231.5	17	60
389	G[202]	4098	316.5	17	60
390	G[204]	4077	231.5	17	60
391	G[206]	4056	316.5	17	60
392	G[208]	4035	231.5	17	60
393	G[210]	4014	316.5	17	60
394	G[212]	3993	231.5	17	60
395	G[214]	3972	316.5	17	60
396	G[216]	3951	231.5	17	60
397	G[218]	3930	316.5	17	60
398	G[220]	3909	231.5	17	60
399	G[222]	3888	316.5	17	60
400	G[224]	3867	231.5	17	60
401	G[226]	3846	316.5	17	60
402	G[228]	3825	231.5	17	60
403	G[230]	3804	316.5	17	60
404	G[232]	3783	231.5	17	60
405	G[234]	3762	316.5	17	60
406	G[236]	3741	231.5	17	60
407	G[238]	3720	316.5	17	60
408	G[240]	3699	231.5	17	60
409	G[242]	3678	316.5	17	60
410	G[244]	3657	231.5	17	60
411	G[246]	3636	316.5	17	60
412	G[248]	3615	231.5	17	60
413	G[250]	3594	316.5	17	60
414	G[252]	3573	231.5	17	60
415	G[254]	3552	316.5	17	60
416	G[256]	3531	231.5	17	60

No.	Name	X-axis	Y-axis	W	H
417	G[258]	3510	316.5	17	60
418	G[260]	3489	231.5	17	60
419	G[262]	3468	316.5	17	60
420	G[264]	3447	231.5	17	60
421	G[266]	3426	316.5	17	60
422	G[268]	3405	231.5	17	60
423	G[270]	3384	316.5	17	60
424	G[272]	3363	231.5	17	60
425	G[274]	3342	316.5	17	60
426	G[276]	3321	231.5	17	60
427	G[278]	3300	316.5	17	60
428	G[280]	3279	231.5	17	60
429	G[282]	3258	316.5	17	60
430	G[284]	3237	231.5	17	60
431	G[286]	3216	316.5	17	60
432	G[288]	3195	231.5	17	60
433	G[290]	3174	316.5	17	60
434	G[292]	3153	231.5	17	60
435	G[294]	3132	316.5	17	60
436	G[296]	3111	231.5	17	60
437	G[298]	3090	316.5	17	60
438	DUMMY[68]	3069	231.5	17	60
439	DUMMY[69]	3048	316.5	17	60
440	DUMMY[70]	3027	231.5	17	60
441	DUMMY[71]	3006	316.5	17	60
442	DUMMY[72]	2985	231.5	17	60
443	DUMMY[73]	2964	316.5	17	60
444	DUMMY[74]	2943	231.5	17	60
445	DUMMY[75]	2835	319	16	65
446	DUMMY[76]	2821	229	16	65
447	VBD[1]	2807	319	16	65
448	S[0]	2793	229	16	65
449	S[1]	2779	319	16	65
450	S[2]	2765	229	16	65
451	S[3]	2751	319	16	65
452	S[4]	2737	229	16	65
453	S[5]	2723	319	16	65
454	S[6]	2709	229	16	65
455	S[7]	2695	319	16	65
456	S[8]	2681	229	16	65
457	S[9]	2667	319	16	65
458	S[10]	2653	229	16	65
459	S[11]	2639	319	16	65
460	S[12]	2625	229	16	65
461	S[13]	2611	319	16	65
462	S[14]	2597	229	16	65
463	S[15]	2583	319	16	65
464	S[16]	2569	229	16	65
465	S[17]	2555	319	16	65
466	S[18]	2541	229	16	65
467	S[19]	2527	319	16	65
468	S[20]	2513	229	16	65
469	S[21]	2499	319	16	65
470	S[22]	2485	229	16	65
471	S[23]	2471	319	16	65
472	S[24]	2457	229	16	65
473	S[25]	2443	319	16	65
474	S[26]	2429	229	16	65
475	S[27]	2415	319	16	65
476	S[28]	2401	229	16	65

No.	Name	X-axis	Y-axis	W	H
477	S[29]	2387	319	16	65
478	S[30]	2373	229	16	65
479	S[31]	2359	319	16	65
480	S[32]	2345	229	16	65
481	S[33]	2331	319	16	65
482	S[34]	2317	229	16	65
483	S[35]	2303	319	16	65
484	S[36]	2289	229	16	65
485	S[37]	2275	319	16	65
486	S[38]	2261	229	16	65
487	S[39]	2247	319	16	65
488	S[40]	2233	229	16	65
489	S[41]	2219	319	16	65
490	S[42]	2205	229	16	65
491	S[43]	2191	319	16	65
492	S[44]	2177	229	16	65
493	S[45]	2163	319	16	65
494	S[46]	2149	229	16	65
495	S[47]	2135	319	16	65
496	S[48]	2121	229	16	65
497	S[49]	2107	319	16	65
498	S[50]	2093	229	16	65
499	S[51]	2079	319	16	65
500	S[52]	2065	229	16	65
501	S[53]	2051	319	16	65
502	S[54]	2037	229	16	65
503	S[55]	2023	319	16	65
504	S[56]	2009	229	16	65
505	S[57]	1995	319	16	65
506	S[58]	1981	229	16	65
507	S[59]	1967	319	16	65
508	S[60]	1953	229	16	65
509	S[61]	1939	319	16	65
510	S[62]	1925	229	16	65
511	S[63]	1911	319	16	65
512	S[64]	1897	229	16	65
513	S[65]	1883	319	16	65
514	S[66]	1869	229	16	65
515	S[67]	1855	319	16	65
516	S[68]	1841	229	16	65
517	S[69]	1827	319	16	65
518	S[70]	1813	229	16	65
519	S[71]	1799	319	16	65
520	S[72]	1785	229	16	65
521	S[73]	1771	319	16	65
522	S[74]	1757	229	16	65
523	S[75]	1743	319	16	65
524	S[76]	1729	229	16	65
525	S[77]	1715	319	16	65
526	S[78]	1701	229	16	65
527	S[79]	1687	319	16	65
528	S[80]	1673	229	16	65
529	S[81]	1659	319	16	65
530	S[82]	1645	229	16	65
531	S[83]	1631	319	16	65
532	S[84]	1617	229	16	65
533	S[85]	1603	319	16	65
534	S[86]	1589	229	16	65
535	S[87]	1575	319	16	65
536	S[88]	1561	229	16	65

No.	Name	X-axis	Y-axis	W	H
537	S[89]	1547	319	16	65
538	S[90]	1533	229	16	65
539	S[91]	1519	319	16	65
540	S[92]	1505	229	16	65
541	S[93]	1491	319	16	65
542	S[94]	1477	229	16	65
543	S[95]	1463	319	16	65
544	S[96]	1449	229	16	65
545	S[97]	1435	319	16	65
546	S[98]	1421	229	16	65
547	S[99]	1407	319	16	65
548	S[100]	1393	229	16	65
549	S[101]	1379	319	16	65
550	S[102]	1365	229	16	65
551	S[103]	1351	319	16	65
552	S[104]	1337	229	16	65
553	S[105]	1323	319	16	65
554	S[106]	1309	229	16	65
555	S[107]	1295	319	16	65
556	S[108]	1281	229	16	65
557	S[109]	1267	319	16	65
558	S[110]	1253	229	16	65
559	S[111]	1239	319	16	65
560	S[112]	1225	229	16	65
561	S[113]	1211	319	16	65
562	S[114]	1197	229	16	65
563	S[115]	1183	319	16	65
564	S[116]	1169	229	16	65
565	S[117]	1155	319	16	65
566	S[118]	1141	229	16	65
567	S[119]	1127	319	16	65
568	S[120]	1113	229	16	65
569	S[121]	1099	319	16	65
570	S[122]	1085	229	16	65
571	S[123]	1071	319	16	65
572	S[124]	1057	229	16	65
573	S[125]	1043	319	16	65
574	S[126]	1029	229	16	65
575	S[127]	1015	319	16	65
576	S[128]	1001	229	16	65
577	S[129]	987	319	16	65
578	S[130]	973	229	16	65
579	S[131]	959	319	16	65
580	S[132]	945	229	16	65
581	S[133]	931	319	16	65
582	S[134]	917	229	16	65
583	S[135]	903	319	16	65
584	S[136]	889	229	16	65
585	S[137]	875	319	16	65
586	S[138]	861	229	16	65
587	S[139]	847	319	16	65
588	S[140]	833	229	16	65
589	S[141]	819	319	16	65
590	S[142]	805	229	16	65
591	S[143]	791	319	16	65
592	S[144]	777	229	16	65
593	S[145]	763	319	16	65
594	S[146]	749	229	16	65
595	S[147]	735	319	16	65
596	S[148]	721	229	16	65

No.	Name	X-axis	Y-axis	W	H
597	S[149]	707	319	16	65
598	S[150]	693	229	16	65
599	S[151]	679	319	16	65
600	S[152]	665	229	16	65
601	S[153]	651	319	16	65
602	S[154]	637	229	16	65
603	S[155]	623	319	16	65
604	S[156]	609	229	16	65
605	S[157]	595	319	16	65
606	S[158]	581	229	16	65
607	S[159]	567	319	16	65
608	S[160]	553	229	16	65
609	S[161]	539	319	16	65
610	S[162]	525	229	16	65
611	S[163]	511	319	16	65
612	S[164]	497	229	16	65
613	S[165]	483	319	16	65
614	S[166]	469	229	16	65
615	S[167]	455	319	16	65
616	S[168]	441	229	16	65
617	S[169]	427	319	16	65
618	S[170]	413	229	16	65
619	S[171]	399	319	16	65
620	S[172]	385	229	16	65
621	S[173]	371	319	16	65
622	S[174]	357	229	16	65
623	S[175]	343	319	16	65
624	S[176]	329	229	16	65
625	S[177]	315	319	16	65
626	S[178]	301	229	16	65
627	S[179]	287	319	16	65
628	S[180]	273	229	16	65
629	S[181]	259	319	16	65
630	S[182]	245	229	16	65
631	S[183]	231	319	16	65
632	S[184]	217	229	16	65
633	S[185]	203	319	16	65
634	S[186]	189	229	16	65
635	S[187]	175	319	16	65
636	S[188]	161	229	16	65
637	S[189]	147	319	16	65
638	S[190]	133	229	16	65
639	S[191]	119	319	16	65
640	S[192]	105	229	16	65
641	S[193]	91	319	16	65
642	S[194]	77	229	16	65
643	S[195]	63	319	16	65
644	S[196]	49	229	16	65
645	S[197]	35	319	16	65
646	S[198]	21	229	16	65
647	S[199]	7	319	16	65
648	S[200]	-7	229	16	65
649	S[201]	-21	319	16	65
650	S[202]	-35	229	16	65
651	S[203]	-49	319	16	65
652	S[204]	-63	229	16	65
653	S[205]	-77	319	16	65
654	S[206]	-91	229	16	65
655	S[207]	-105	319	16	65
656	S[208]	-119	229	16	65

No.	Name	X-axis	Y-axis	W	H
657	S[209]	-133	319	16	65
658	S[210]	-147	229	16	65
659	S[211]	-161	319	16	65
660	S[212]	-175	229	16	65
661	S[213]	-189	319	16	65
662	S[214]	-203	229	16	65
663	S[215]	-217	319	16	65
664	S[216]	-231	229	16	65
665	S[217]	-245	319	16	65
666	S[218]	-259	229	16	65
667	S[219]	-273	319	16	65
668	S[220]	-287	229	16	65
669	S[221]	-301	319	16	65
670	S[222]	-315	229	16	65
671	S[223]	-329	319	16	65
672	S[224]	-343	229	16	65
673	S[225]	-357	319	16	65
674	S[226]	-371	229	16	65
675	S[227]	-385	319	16	65
676	S[228]	-399	229	16	65
677	S[229]	-413	319	16	65
678	S[230]	-427	229	16	65
679	S[231]	-441	319	16	65
680	S[232]	-455	229	16	65
681	S[233]	-469	319	16	65
682	S[234]	-483	229	16	65
683	S[235]	-497	319	16	65
684	S[236]	-511	229	16	65
685	S[237]	-525	319	16	65
686	S[238]	-539	229	16	65
687	S[239]	-553	319	16	65
688	S[240]	-567	229	16	65
689	S[241]	-581	319	16	65
690	S[242]	-595	229	16	65
691	S[243]	-609	319	16	65
692	S[244]	-623	229	16	65
693	S[245]	-637	319	16	65
694	S[246]	-651	229	16	65
695	S[247]	-665	319	16	65
696	S[248]	-679	229	16	65
697	S[249]	-693	319	16	65
698	S[250]	-707	229	16	65
699	S[251]	-721	319	16	65
700	S[252]	-735	229	16	65
701	S[253]	-749	319	16	65
702	S[254]	-763	229	16	65
703	S[255]	-777	319	16	65
704	S[256]	-791	229	16	65
705	S[257]	-805	319	16	65
706	S[258]	-819	229	16	65
707	S[259]	-833	319	16	65
708	S[260]	-847	229	16	65
709	S[261]	-861	319	16	65
710	S[262]	-875	229	16	65
711	S[263]	-889	319	16	65
712	S[264]	-903	229	16	65
713	S[265]	-917	319	16	65
714	S[266]	-931	229	16	65
715	S[267]	-945	319	16	65
716	S[268]	-959	229	16	65

No.	Name	X-axis	Y-axis	W	H
717	S[269]	-973	319	16	65
718	S[270]	-987	229	16	65
719	S[271]	-1001	319	16	65
720	S[272]	-1015	229	16	65
721	S[273]	-1029	319	16	65
722	S[274]	-1043	229	16	65
723	S[275]	-1057	319	16	65
724	S[276]	-1071	229	16	65
725	S[277]	-1085	319	16	65
726	S[278]	-1099	229	16	65
727	S[279]	-1113	319	16	65
728	S[280]	-1127	229	16	65
729	S[281]	-1141	319	16	65
730	S[282]	-1155	229	16	65
731	S[283]	-1169	319	16	65
732	S[284]	-1183	229	16	65
733	S[285]	-1197	319	16	65
734	S[286]	-1211	229	16	65
735	S[287]	-1225	319	16	65
736	S[288]	-1239	229	16	65
737	S[289]	-1253	319	16	65
738	S[290]	-1267	229	16	65
739	S[291]	-1281	319	16	65
740	S[292]	-1295	229	16	65
741	S[293]	-1309	319	16	65
742	S[294]	-1323	229	16	65
743	S[295]	-1337	319	16	65
744	S[296]	-1351	229	16	65
745	S[297]	-1365	319	16	65
746	S[298]	-1379	229	16	65
747	S[299]	-1393	319	16	65
748	S[300]	-1407	229	16	65
749	S[301]	-1421	319	16	65
750	S[302]	-1435	229	16	65
751	S[303]	-1449	319	16	65
752	S[304]	-1463	229	16	65
753	S[305]	-1477	319	16	65
754	S[306]	-1491	229	16	65
755	S[307]	-1505	319	16	65
756	S[308]	-1519	229	16	65
757	S[309]	-1533	319	16	65
758	S[310]	-1547	229	16	65
759	S[311]	-1561	319	16	65
760	S[312]	-1575	229	16	65
761	S[313]	-1589	319	16	65
762	S[314]	-1603	229	16	65
763	S[315]	-1617	319	16	65
764	S[316]	-1631	229	16	65
765	S[317]	-1645	319	16	65
766	S[318]	-1659	229	16	65
767	S[319]	-1673	319	16	65
768	S[320]	-1687	229	16	65
769	S[321]	-1701	319	16	65
770	S[322]	-1715	229	16	65
771	S[323]	-1729	319	16	65
772	S[324]	-1743	229	16	65
773	S[325]	-1757	319	16	65
774	S[326]	-1771	229	16	65
775	S[327]	-1785	319	16	65
776	S[328]	-1799	229	16	65

No.	Name	X-axis	Y-axis	W	H
777	S[329]	-1813	319	16	65
778	S[330]	-1827	229	16	65
779	S[331]	-1841	319	16	65
780	S[332]	-1855	229	16	65
781	S[333]	-1869	319	16	65
782	S[334]	-1883	229	16	65
783	S[335]	-1897	319	16	65
784	S[336]	-1911	229	16	65
785	S[337]	-1925	319	16	65
786	S[338]	-1939	229	16	65
787	S[339]	-1953	319	16	65
788	S[340]	-1967	229	16	65
789	S[341]	-1981	319	16	65
790	S[342]	-1995	229	16	65
791	S[343]	-2009	319	16	65
792	S[344]	-2023	229	16	65
793	S[345]	-2037	319	16	65
794	S[346]	-2051	229	16	65
795	S[347]	-2065	319	16	65
796	S[348]	-2079	229	16	65
797	S[349]	-2093	319	16	65
798	S[350]	-2107	229	16	65
799	S[351]	-2121	319	16	65
800	S[352]	-2135	229	16	65
801	S[353]	-2149	319	16	65
802	S[354]	-2163	229	16	65
803	S[355]	-2177	319	16	65
804	S[356]	-2191	229	16	65
805	S[357]	-2205	319	16	65
806	S[358]	-2219	229	16	65
807	S[359]	-2233	319	16	65
808	S[360]	-2247	229	16	65
809	S[361]	-2261	319	16	65
810	S[362]	-2275	229	16	65
811	S[363]	-2289	319	16	65
812	S[364]	-2303	229	16	65
813	S[365]	-2317	319	16	65
814	S[366]	-2331	229	16	65
815	S[367]	-2345	319	16	65
816	S[368]	-2359	229	16	65
817	S[369]	-2373	319	16	65
818	S[370]	-2387	229	16	65
819	S[371]	-2401	319	16	65
820	S[372]	-2415	229	16	65
821	S[373]	-2429	319	16	65
822	S[374]	-2443	229	16	65
823	S[375]	-2457	319	16	65
824	S[376]	-2471	229	16	65
825	S[377]	-2485	319	16	65
826	S[378]	-2499	229	16	65
827	S[379]	-2513	319	16	65
828	S[380]	-2527	229	16	65
829	S[381]	-2541	319	16	65
830	S[382]	-2555	229	16	65
831	S[383]	-2569	319	16	65
832	S[384]	-2583	229	16	65
833	S[385]	-2597	319	16	65
834	S[386]	-2611	229	16	65
835	S[387]	-2625	319	16	65
836	S[388]	-2639	229	16	65

No.	Name	X-axis	Y-axis	W	H
837	S[389]	-2653	319	16	65
838	S[390]	-2667	229	16	65
839	S[391]	-2681	319	16	65
840	S[392]	-2695	229	16	65
841	S[393]	-2709	319	16	65
842	S[394]	-2723	229	16	65
843	S[395]	-2737	319	16	65
844	S[396]	-2751	229	16	65
845	S[397]	-2765	319	16	65
846	S[398]	-2779	229	16	65
847	S[399]	-2793	319	16	65
848	VBD[2]	-2807	229	16	65
849	DUMMY[77]	-2821	319	16	65
850	DUMMY[78]	-2835	229	16	65
851	DUMMY[79]	-2943	316.5	17	60
852	DUMMY[80]	-2964	231.5	17	60
853	DUMMY[81]	-2985	316.5	17	60
854	DUMMY[82]	-3006	231.5	17	60
855	DUMMY[83]	-3027	316.5	17	60
856	DUMMY[84]	-3048	231.5	17	60
857	DUMMY[85]	-3069	316.5	17	60
858	G[299]	-3090	231.5	17	60
859	G[297]	-3111	316.5	17	60
860	G[295]	-3132	231.5	17	60
861	G[293]	-3153	316.5	17	60
862	G[291]	-3174	231.5	17	60
863	G[289]	-3195	316.5	17	60
864	G[287]	-3216	231.5	17	60
865	G[285]	-3237	316.5	17	60
866	G[283]	-3258	231.5	17	60
867	G[281]	-3279	316.5	17	60
868	G[279]	-3300	231.5	17	60
869	G[277]	-3321	316.5	17	60
870	G[275]	-3342	231.5	17	60
871	G[273]	-3363	316.5	17	60
872	G[271]	-3384	231.5	17	60
873	G[269]	-3405	316.5	17	60
874	G[267]	-3426	231.5	17	60
875	G[265]	-3447	316.5	17	60
876	G[263]	-3468	231.5	17	60
877	G[261]	-3489	316.5	17	60
878	G[259]	-3510	231.5	17	60
879	G[257]	-3531	316.5	17	60
880	G[255]	-3552	231.5	17	60
881	G[253]	-3573	316.5	17	60
882	G[251]	-3594	231.5	17	60
883	G[249]	-3615	316.5	17	60
884	G[247]	-3636	231.5	17	60
885	G[245]	-3657	316.5	17	60
886	G[243]	-3678	231.5	17	60
887	G[241]	-3699	316.5	17	60
888	G[239]	-3720	231.5	17	60
889	G[237]	-3741	316.5	17	60
890	G[235]	-3762	231.5	17	60
891	G[233]	-3783	316.5	17	60
892	G[231]	-3804	231.5	17	60
893	G[229]	-3825	316.5	17	60
894	G[227]	-3846	231.5	17	60
895	G[225]	-3867	316.5	17	60
896	G[223]	-3888	231.5	17	60

No.	Name	X-axis	Y-axis	W	H
897	G[221]	-3909	316.5	17	60
898	G[219]	-3930	231.5	17	60
899	G[217]	-3951	316.5	17	60
900	G[215]	-3972	231.5	17	60
901	G[213]	-3993	316.5	17	60
902	G[211]	-4014	231.5	17	60
903	G[209]	-4035	316.5	17	60
904	G[207]	-4056	231.5	17	60
905	G[205]	-4077	316.5	17	60
906	G[203]	-4098	231.5	17	60
907	G[201]	-4119	316.5	17	60
908	G[199]	-4140	231.5	17	60
909	G[197]	-4161	316.5	17	60
910	G[195]	-4182	231.5	17	60
911	G[193]	-4203	316.5	17	60
912	G[191]	-4224	231.5	17	60
913	G[189]	-4245	316.5	17	60
914	G[187]	-4266	231.5	17	60
915	G[185]	-4287	316.5	17	60
916	G[183]	-4308	231.5	17	60
917	G[181]	-4329	316.5	17	60
918	G[179]	-4350	231.5	17	60
919	G[177]	-4371	316.5	17	60
920	G[175]	-4392	231.5	17	60
921	G[173]	-4413	316.5	17	60
922	G[171]	-4434	231.5	17	60
923	G[169]	-4455	316.5	17	60
924	G[167]	-4476	231.5	17	60
925	G[165]	-4497	316.5	17	60
926	G[163]	-4518	231.5	17	60
927	G[161]	-4539	316.5	17	60
928	G[159]	-4560	231.5	17	60
929	G[157]	-4581	316.5	17	60
930	G[155]	-4602	231.5	17	60
931	G[153]	-4623	316.5	17	60
932	G[151]	-4644	231.5	17	60
933	G[149]	-4665	316.5	17	60
934	G[147]	-4686	231.5	17	60
935	G[145]	-4707	316.5	17	60
936	G[143]	-4728	231.5	17	60
937	G[141]	-4749	316.5	17	60
938	G[139]	-4770	231.5	17	60
939	G[137]	-4791	316.5	17	60
940	G[135]	-4812	231.5	17	60
941	G[133]	-4833	316.5	17	60
942	G[131]	-4854	231.5	17	60
943	G[129]	-4875	316.5	17	60
944	G[127]	-4896	231.5	17	60
945	G[125]	-4917	316.5	17	60
946	G[123]	-4938	231.5	17	60
947	G[121]	-4959	316.5	17	60
948	G[119]	-4980	231.5	17	60
949	G[117]	-5001	316.5	17	60
950	G[115]	-5022	231.5	17	60
951	G[113]	-5043	316.5	17	60
952	G[111]	-5064	231.5	17	60
953	G[109]	-5085	316.5	17	60
954	G[107]	-5106	231.5	17	60
955	G[105]	-5127	316.5	17	60
956	G[103]	-5148	231.5	17	60

No.	Name	X-axis	Y-axis	W	H
957	G[101]	-5169	316.5	17	60
958	G[99]	-5190	231.5	17	60
959	G[97]	-5211	316.5	17	60
960	G[95]	-5232	231.5	17	60
961	G[93]	-5253	316.5	17	60
962	G[91]	-5274	231.5	17	60
963	G[89]	-5295	316.5	17	60
964	G[87]	-5316	231.5	17	60
965	G[85]	-5337	316.5	17	60
966	G[83]	-5358	231.5	17	60
967	G[81]	-5379	316.5	17	60
968	G[79]	-5400	231.5	17	60
969	G[77]	-5421	316.5	17	60
970	G[75]	-5442	231.5	17	60
971	G[73]	-5463	316.5	17	60
972	G[71]	-5484	231.5	17	60
973	G[69]	-5505	316.5	17	60
974	G[67]	-5526	231.5	17	60
975	G[65]	-5547	316.5	17	60
976	G[63]	-5568	231.5	17	60
977	G[61]	-5589	316.5	17	60
978	G[59]	-5610	231.5	17	60
979	G[57]	-5631	316.5	17	60
980	G[55]	-5652	231.5	17	60
981	G[53]	-5673	316.5	17	60
982	G[51]	-5694	231.5	17	60
983	G[49]	-5715	316.5	17	60
984	G[47]	-5736	231.5	17	60
985	G[45]	-5757	316.5	17	60
986	G[43]	-5778	231.5	17	60
987	G[41]	-5799	316.5	17	60
988	G[39]	-5820	231.5	17	60
989	G[37]	-5841	316.5	17	60
990	G[35]	-5862	231.5	17	60
991	G[33]	-5883	316.5	17	60
992	G[31]	-5904	231.5	17	60
993	G[29]	-5925	316.5	17	60
994	G[27]	-5946	231.5	17	60
995	G[25]	-5967	316.5	17	60
996	G[23]	-5988	231.5	17	60
997	G[21]	-6009	316.5	17	60
998	G[19]	-6030	231.5	17	60
999	G[17]	-6051	316.5	17	60
1000	G[15]	-6072	231.5	17	60
1001	G[13]	-6093	316.5	17	60
1002	G[11]	-6114	231.5	17	60
1003	G[9]	-6135	316.5	17	60
1004	G[7]	-6156	231.5	17	60
1005	G[5]	-6177	316.5	17	60
1006	G[3]	-6198	231.5	17	60
1007	G[1]	-6219	316.5	17	60
1008	DUMMY[86]	-6240	231.5	17	60
1009	DUMMY[87]	-6261	316.5	17	60
1010	DUMMY[88]	-6282	231.5	17	60
1011	DUMMY[89]	-6303	316.5	17	60
1012	DUMMY[90]	-6324	231.5	17	60
1013	DUMMY[91]	-6345	316.5	17	60

13. REVISION HISTORY

Revision	Content	Page	Date
1.0.1	JD79660 datasheet 1st version	-	2023/06/06
1.0.2	Updated Cascade Register	-	2023/06/13
1.0.3	Updated Bump Information		2023/06/14
1.0.4	Updated Bump Information		2023/06/20