

SSD2681

Advance information

**200 Source x 200 Gate
Active Matrix EPD Display Driver with Controller
for color application**

SSD2681 products shall only be used solely with Permitted E5 Spectra 3100 FPL licensed by E Ink, customer should notify the same acknowledgement with its downstream customers.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: Revision history

Revision	Description of any change	Effective
SSD2681 Advance Information 1.0	Initial release Advance Information 1.0	16-Oct-2025

GOOD DISPLAY

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CONTENTS

1	GENERAL DESCRIPTION	5
2	FEATURES.....	5
3	ORDERING INFORMATION	6
4	BLOCK DIAGRAM	6
5	PIN DESCRIPTION	7
6	FUNCTIONAL BLOCK DESCRIPTION.....	9
6.1	MCU INTERFACE	9
6.2	MCU INTERFACE SELECTION	9
6.3	MCU SERIAL INTERFACE (4-WIRE SPI).....	9
6.4	MCU SERIAL PERIPHERAL INTERFACE (3-WIRE SPI)	10
6.5	RAM	10
6.6	OSCILLATOR.....	10
6.7	BOOSTER & REGULATOR	10
6.8	VCOM SENSING	10
7	COMMAND TABLE.....	11
7.1	USER COMMAND TABLE	11
8	COMMAND TABLE DESCRIPTION	13
9	DISPLAY ON/OFF SEQUENCE.....	27
9.1	DISPLAY ON SEQUENCE FROM VDD POWER ON.....	27
9.2	DISPLAY ON SEQUENCE FROM DEEP SLEEP MODE	28
9.3	DISPLAY OFF SEQUENCE DISPLAY	28
10	ABSOLUTE MAXIMUM RATING	29
11	ELECTRICAL CHARACTERISTICS	29
12	AC CHARACTERISTICS.....	31
12.1	SERIAL PERIPHERAL INTERFACE	31
13	APPLICATION CIRCUIT	33
14	PACKAGE INFORMATION.....	34
14.1	DIE TRAY DIMENSIONS FOR SSD2681Z2 / SSD2681ZA	34

TABLES

TABLE 3-1 : ORDERING INFORMATION.....	6
TABLE 5-1: POWER SUPPLY PINS	7
TABLE 5-2: INTERFACE LOGIC PINS	7
TABLE 5-3: ANALOG PINS.....	8
TABLE 5-4: DRIVER OUTPUT PINS.....	8
TABLE 5-5: OTHER PINS.....	8
TABLE 6-1: INTERFACE PINS ASSIGNMENT UNDER DIFFERENT MCU INTERFACE	9
TABLE 6-2: CONTROL PINS STATUS OF 4-WIRE SPI.....	9
TABLE 6-3: CONTROL PINS STATUS OF 3-WIRE SPI.....	10
TABLE 7-1: SUMMARY OF USER COMMAND TABLE.....	11
TABLE 10-1 : MAXIMUM RATINGS	29
TABLE 11-1: DC CHARACTERISTICS	29
TABLE 12-1 : SERIAL PERIPHERAL INTERFACE TIMING CHARACTERISTICS.....	31
TABLE 13-1: COMPONENT LIST FOR SSD2681 APPLICATION CIRCUIT	33

FIGURES

FIGURE 4-1 : SSD2681 BLOCK DIAGRAM.....	6
FIGURE 6-1 : READ/WRITE PROCEDURE IN 4-WIRE SPI MODE.....	9
FIGURE 6-2 : READ/WRITE PROCEDURE IN 3-WIRE SPI MODE	10
FIGURE 12-1: 3-WIRE SPI CHARACTERISTICS (WRITE MODE).....	31
FIGURE 12-2: 3-WIRE SPI CHARACTERISTICS (READ MODE)	31
FIGURE 12-3: 4-WIRE SPI CHARACTERISTICS (WRITE MODE).....	32
FIGURE 12-4: 4-WIRE SPI CHARACTERISTICS (READ MODE).....	32
FIGURE 13-1: SSD2681 APPLICATION CIRCUIT	33
FIGURE 14-1: SSD2681Z2 / SSD2681ZA DIE TRAY INFORMATION (UNIT: MM).....	34

1 General Description

The SSD2681 is an all-in-one AMEPD driver IC with Controller which can support EPD color application.

It consists of 200 source outputs, 200 gate outputs, 1 VCOM & 1 VBD which can support a maximum display resolution 200x200.

SSD2681 embeds oscillator, booster & regulators and selectable Serial Peripheral Interface (3-wire/4-wire) to communicate with general MCU.

2 Features

- Design for dot matrix type active matrix EPD display, support Black/White/Color
- Power supply:
 - VDD: 2.2V to 3.6V
 - VDDIO: Connect to VDD
- On chip display RAM
 - 2bit outputs per pixel to support Black/White/Color
- Resolution: 200 gate outputs, 200 source outputs, 1VBD (for border) and 1 VCOM
 - 200 output gate drivers:
 - 2-level outputs (VGH, VGL), Max 40Vp-p
 - Gate driving output voltage (VGH/VGL): +/-20V, +/-17V, +/-15V
 - Up and Down shift capability
 - 200 output source drivers with 4 levels output for black/white/color per pixel:
 - Mode 0 & 1 can be switched frame by frame (panel scanning frame):
 - Mode 0: 0V & VSH1 (+15V) & VSL (-15V) & VSH2 (+3V to +15V)
 - Mode 1: 0V & VSH1 (+3V to +15V) & VSL (-3V to -15V) & VSH2 (+3V to +15V)
 - **VSH1 should be always >= VSH2**
 - Source driving output voltage (Voltage step: 200mV)
 - Left and Right shift capability
 - 1 VBD for border level
 - Same function as the programmable source driver with selected LUT
 - 4 levels output (DCVCOM, VSH1, VSL and VSH2)
 - 1 VCOM for Common electrode level
 - DCVCOM: -0.2V to -3V (Voltage step: 200mV)
 - ACVCOM: 4 levels output (DCVCOM, VSH1+DCVCOM, VSL+DCVCOM and floating)
 - Built in VCOM sensing.
- On-chip oscillator
- Programmable output Waveform Settings
- Support frame rate: 120Hz (max)
- External or internal generated voltage for MTP
- Embedded 4k Bytes MTP to store the waveform settings and parameters.
- Support low voltage detect for supply voltage.
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC, 7-bit status
- MCU interface: Serial peripheral (3-wire/4-wire), Maximum SPI write speed 20MHz
- Available in COG package

3 Ordering Information

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD2681Z2	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 9um
SSD2681ZA	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 9um

4 Block Diagram

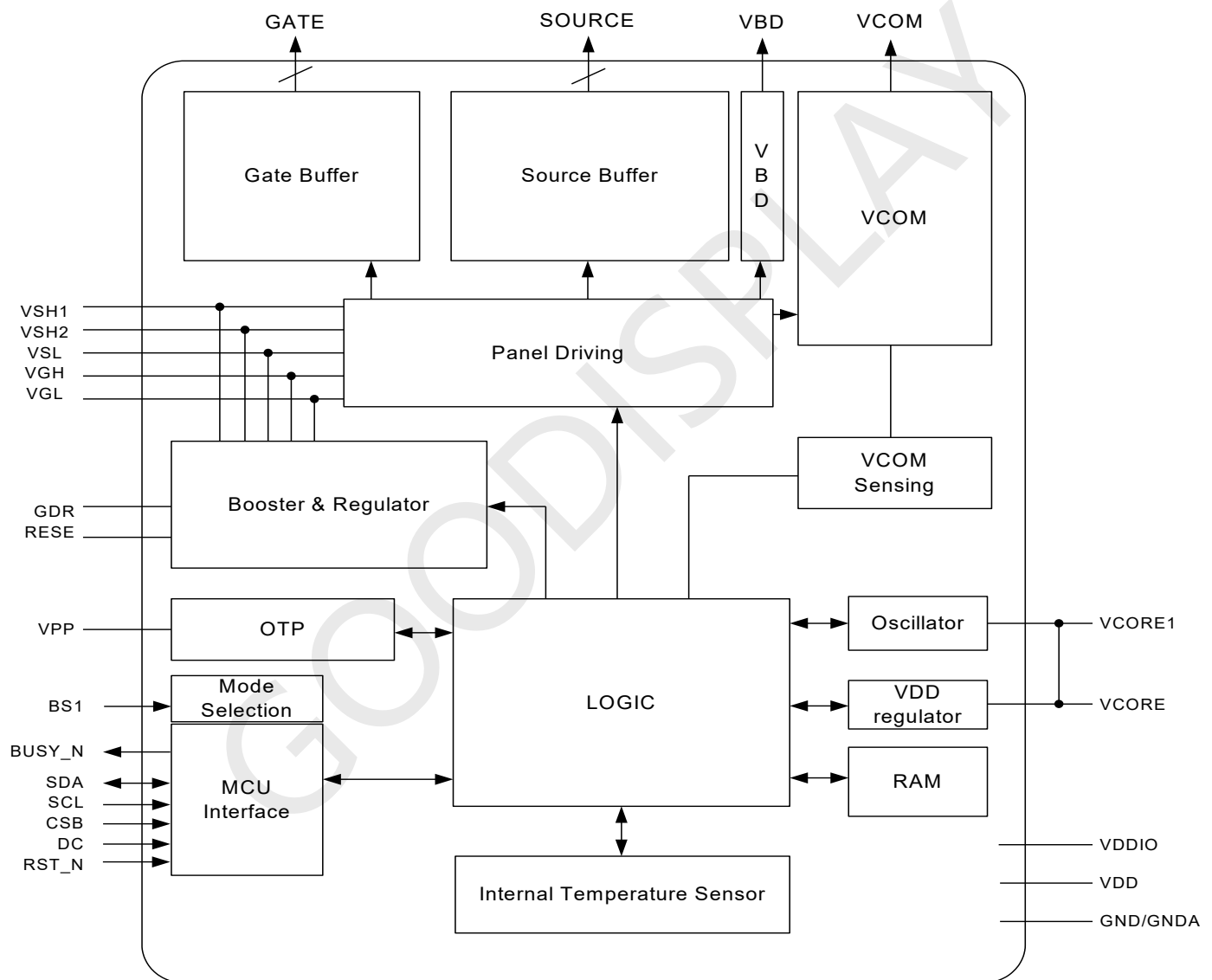


Figure 4-1 : SSD2681 Block Diagram

SSD2681 products shall only be used solely with Permitted E5 Spectra 3100 FPL licensed by E Ink, customer should notify the same acknowledgement with its downstream customers.

5 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to GND, Pull H = connect to V_{DDIO}

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VDD	P	Power Supply	Power Supply	Power input pin for the chip.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the interface. - Connect to VDD in the application circuit.	-
VCORE	C	Capacitor	Logic Power	Core logic power pin. VCORE is regulated internally from VDD.	-
VCORE1	C	Capacitor	Logic Power	Core logic power pin1. - connect to VCORE in the application circuit	-
GND	P	GND	GND	Ground	-
GNDA	P	GND	GND	Ground - Connect to GND in the application circuit	-
VPP	P	Reserved	Reserved	Reserved Keep it floating.	-

Table 5-2: Interface Logic Pins

Name	Type	Connect to	Function	Description		When not in use
BS1	I	VDDIO/GND	MCU Interface Mode Selection	This pin is for selecting 3-wire or 4-wire SPI bus.		-
				BS1	MCU Interface	
				0	4-wire SPI	
				1	3-wire SPI(9 bits SPI)	
SCL	I	MPU	Data Bus	Serial clock pin for interface		-
SDA	I/O	MPU	Data Bus	Serial data pin for interface		-
CSB	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU.		-
DC	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU.		VDDIO or GND
RST_N	I	MPU	System Reset	This pin is reset signal input. Active Low.		-
BUSY_N	O	MPU	Device Busy Signal	This pin indicates the driver status. L: Driver is busy H: non-busy. Host side can send command/data to driver.		Open

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	MOSFET Driver	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and GND in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and GND in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1. Connect a stabilizing capacitor between VSH1 and GND in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2. Connect a stabilizing capacitor between VSH2 and GND in the application circuit.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL. Connect a stabilizing capacitor between VSL and GND in the application circuit.	-
VCOM	C	Panel & Stabilizing capacitor	VCOM driving signal	This pin is VCOM driving voltage, VCOM. Connect a stabilizing capacitor between VCOM and GND in the application circuit.	-

Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [199:0]	O	Panel	Source driving signal	Source output pin.	Open
G [199:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open

Table 5-5: Other Pins

Name	Type	Connect to	Function	Description	When not in use
TIN	I	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
TPE	O	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
CL	I/O	Open	Reserved	Reserved	Open
RSV	NC	NC	Reserved	This is a reserved pin and should be kept open.	Open
TPA, TPB, TPC, TPF	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPE, TPF, TIN	Open
NC	NC	NC	NC	Do not connect.	

6 Functional Block Description

6.1 MCU Interface

6.2 MCU Interface selection

The SSD2681 can support 3-wire/4-wire serial peripheral. In the SSD2681, the MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1: Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	DC	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

6.3 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C and CSB. The control pins status in 4-wire SPI in reading/writing command/data is shown in Table 6-2: Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

. The read/write procedure of 4-wire SPI is shown in Figure 6-1.

Table 6-2: Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to DC pin.

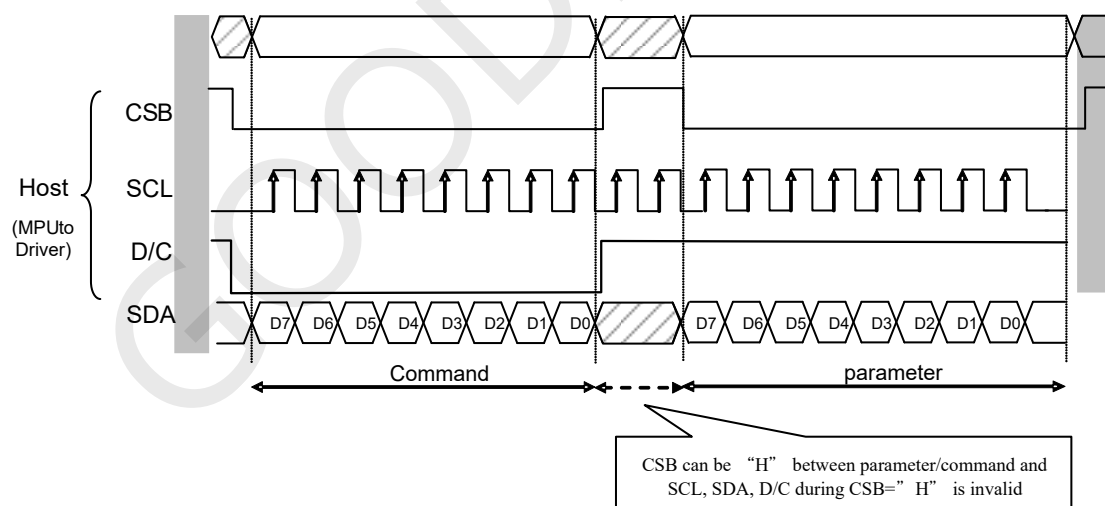


Figure 6-1 : Read/Write procedure in 4-wire SPI mode

6.4 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while DC pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3. The read/write procedure of 3-wire SPI is shown in Figure 6-2.

In the read/write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C bit, D7 bit, D6 bit to D0 bit. The first bit is DC bit which determines the following byte is command or data. When DC bit is 0, the following byte is command. When DC bit is 1, the following byte is data. Figure 6-2 shows the write procedure in 3-wire SPI

Table 6-3: Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

Note:

- (1) L is connected to GND and H is connected to VDDIO
- (2) ↑ stands for rising edge of signal

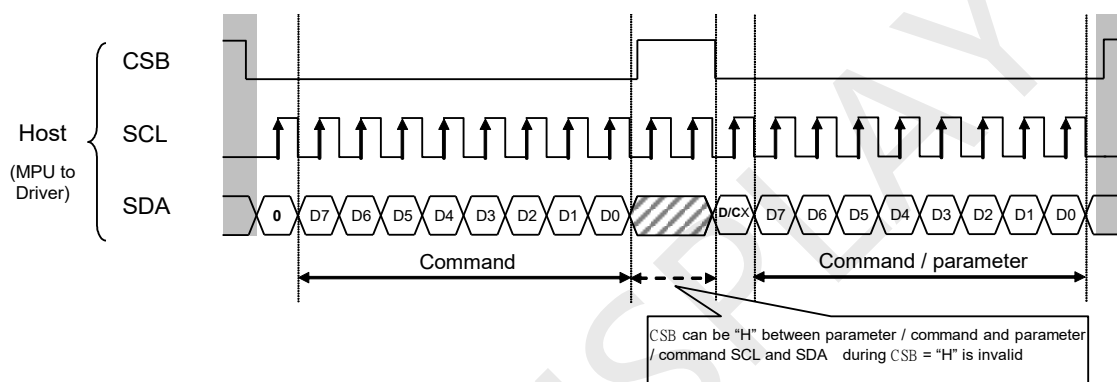


Figure 6-2 : Read/Write procedure in 3-wire SPI mode

6.5 RAM

The On chip display RAM is holding the image data. 2bpp for 200x200 resolution

6.6 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

6.7 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

6.8 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into MTP. It required PON with DCVCOM mode for analog voltage ready.

The typical flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are GND.
- VCOM pin is used for sensing.
- During Sensing period, BUSY_N is kept flagged.
- After Sensing, Active Gate return to non-select stage.

7 COMMAND TABLE

7.1 User Command Table

Table 7-1: Summary of user command table

R/W#	DC	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR	
W	0	00h	PSR Panel Setting Register	0	0	0	0	0	0	0	0		
W	1			RES[1:0]		B mode	0	UD	SHL	SHD_N	RST_N	2Fh	
W	1			LUT_EN	FOPT[1:0]		VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h	
W	0	01h	PWR Power setting Register	0	0	0	0	0	0	0	1		
W	1			0	0	0	0	0	VSC_EN	VS_EN	VG_EN	07h	
W	1			1	1	1	1	0	VGPN[1:0]			F0h	
W	1			VSPL[6:0]									00h
W	1			VSNL[6:0]									00h
W	1			VSPL2[6:0]									00h
W	1			VSNL2[6:0]									00h
W	0	02h	POF Power OFF Command Register	0	0	0	0	0	0	1	0		
W	1			00h									
W	0	03h	POFS Power off Sequence Setting Register	0	0	0	0	0	0	1	1		
W	1			T_VDPG_OFF[1:0]		0	0	T_VDS_OFF[1:0]			00h		
W	0	04h	PON Power ON Command Register	0	0	0	0	0	1	0	0		
W	0			0	0	0	0	1	1	0			
W	1	06h	BTST Booster Soft Start Setting Register	0	VGHSCT_ONT[2:0]			T_VGHSSA[1:0]		T_VGHSSB[1:0]		0Fh	
W	1			1	VGHSCT_DRV[2:0]			VGHSCT_OFFT[3:0]				8Bh	
W	1			1	VGHSCT_DRV[2:0]			VGHSCT_OFFT[3:0]				9Ch	
W	1			1	VGHSCT_DRV[2:0]			VGHSCT_OFFT[3:0]				96h	
W	0	07h	DSLTP Deep Sleep Register	0	0	0	0	0	1	1	1		
W	1			A5h									
W	0	10h	DTM Data Start transmission Register	0	0	0	1	0	0	0	0		
W	1			KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		-	
W	1			KPixel(4M-3)[1:0]		KPixel(4M-2)[1:0]		KPixel(4M-1)[1:0]		KPixel(4M)[1:0]		-	
W	1			KPixel(4M-3)[1:0]		KPixel(4M-2)[1:0]		KPixel(4M-1)[1:0]		KPixel(4M)[1:0]		-	
W	0	12h	DRF Display Refresh Command Register	0	0	0	1	0	0	1	0		
W	1			00h									
W	0	17h	AUTO Auto Sequence Register	0	0	0	1	0	1	1	1		
W	1			A5h or A7h									
W	0	30h	PLL Frame Rate Control register	0	0	1	1	0	0	0	0		
W	1			0	0	0	0	DYNA	FR[2:0]			02h	
W	0	40h	TSC Temperature Sensor Command Register	0	1	0	0	0	0	0	0		
R	1			TS[7:0]									
W	0	41h	TSE Temperature Sensor Enable Register	0	1	0	0	0	0	0	1		
W	1			0	0	0	0	TO[3:1]		0		00h	
W	0	50h	CDI VCOM and DATA interval setting Register	0	1	0	1	0	0	0	0		
W	1			VBD[2:0]			DDX	CDI[3:0]				97h	
W	0	51h	LPD Lower Power Detection Register	0	1	0	1	0	0	0	1		
R	1			0	0	0	0	0	0	LPDstatus			
W	0	61h	TRES Resolution setting Register	0	1	1	0	0	0	0	1		
W	1			0	0	0	0	0	0	0		00h	
W	1			HRES[7:0]									C8h
W	1			0	0	0	0	0	0	0	0		00h
W	1	62h	HTOTAL	VRES[7:0]									C8h
W	0			0	1	1	0	0	0	1	0		
W	1			HTOTAL_A[7:0]									64h
W	1			HTOTAL_B[7:0]									53h
W	0	65h	GSST Gate/Source Start Setting Register	0	1	1	0	0	1	0	1		
W	1			0	0	0	0	0	0	0		00h	
W	1			S_start[7:0]									00h
W	1			0	0	0	0	0	0	0	0		00h
W	1	65h	GSST Gate/Source Start Setting Register	G_start[7:0]									00h
W	1			G_start[7:0]									00h

R/W#	DC	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR
W	0	70h	REV Chip Revision Register	0	1	1	1	0	0	0	0	
R	1			A[7:0]							48h	
R	1			B[7:0]							01h	
R	1			C[7:0]							01h	
W	0	80h	AMV Auto Measurement VCOM Register	1	0	0	0	0	0	0	0	
W	1			P[1:0]		AMVT[1:0]		AMVX	AMVS	0	AMVE	00h
W	0	81h	VV VCOM Value Register	1	0	0	0	0	0	0	1	
R	1			VV[5:0]							-	
W	0	82h	VDCS VCM_DC Setting Register	1	0	0	0	0	0	1	0	
W	1			MTP_VCM	VDCS[6:0]							00h
W	0	83h	PTLW PARTIAL WINDOW	1	0	0	0	0	0	1	1	
W	1			0	0	0	0	0	0	0	0	00h
W	1			HRST[7:0]							00h	
W	1			0	0	0	0	0	0	0	0	00h
W	1			HRED[7:0]							C7h	
W	1			0	0	0	0	0	0	0	0	00h
W	1			VRST[7:0]							00h	
W	1			0	0	0	0	0	0	0	0	00h
W	1			VRED[7:0]							C7h	
W	1			0	0	0	0	0	0	0	PMODE	00h
W	0	90h	PGM Program Mode	1	0	0	1	0	0	0	0	
W	0	91h	APG Active Program	1	0	0	1	0	0	0	1	
W	0	92h	RMTP Read MTP Data	1	0	0	1	0	0	1	0	
R	1			dummy byte							-	
R	1			Address 0 in MTP							-	
R	1			...							...	
R	1	Address n in MTP							-			
W	0	A2h	PWS_CFG	1	0	1	0	0	0	1	0	
W	1			0	0	1	1	0	PGM_UMODE[2:0]		31h	
W	1			0	PGM_SADDR[15:8]							00h
W	1			0	PGM_SADDR[7:0]							00h
W	1			0	PGM_DSIZE[15:8]							00h
W	1			0	PGM_DSIZE[7:0]							00h
W	0	A3h	PGM_STAT	1	0	1	0	0	0	1	1	
R	1			0	0	0	0	0	0	PGM_VER_ERR	PGM_EXE_ERR	-
W	0	A4h	FTP_STAT	1	0	1	0	0	1	0	0	
R	1			0	0	0	0	0	0	LUT_TYPE[1:0]		00h
R	1			0	0	0	0	0	Free_BLK[3:0]		00h	
R	1			FREE_UI[7:0]							00h	
W	0	E0h	CCSET Temperature input selection	1	1	1	0	0	0	0	0	
W	1			0	0	0	0	0	0	TSFIX	0	00h
W	0	E3h	PWS Power Saving Register	1	1	1	0	0	0	1	1	
W	1			VCOM_W[3:0]				SD_W[3:0]				65h
W	0	E4h	LVSEL LVD Voltage Select Register	1	1	1	0	0	1	0	0	
W	1			0	0	0	0	0	0	LVD_SEL[1:0]		03h
W	0	E6h	TSSET Manual input temperature value	1	1	1	0	0	1	1	0	
W	1			TS_SET[7:0]							00h	
W	0	E7h	PST	1	1	1	0	0	1	1	1	
W	1			0	VGHSM_DRV[2:0]				VGHSM_OFFT[3:0]			

Note:

- (1) The bit which has been written as "0" or "1" in Table 7-1 must be followed. Otherwise, device malfunction may occur.
- (2) The driver IC will not response to all read & write commands during BUSY_N=0.
- (3) Commands are only effective while all corresponding parameters for that command were written completely.
- (4) Commands or parameters not shown on above table are for "Reserve" usage.
- (5) POR value may be changed without notice.

8 Command Table Description

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register
0	1		A ₇	A ₆	A ₅	0	A ₃	A ₂	A ₁	A ₀		A[7:0] = 2Fh [POR] B[7:0] = 09h [POR] A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: 200 x 200 (Default) 01b: 152 x 152 10b: 104 x 104 11b: 160 x 160 *Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power. A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 ... G0 1: Scan up. (Default) First line to Last line: G0 ... Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 ... S0 1: Shift right. (Default) First data to Last data: S0 ... Sn-1 A[1] ~ SHD_N Booster Switch: 0 : Booster off, register data are kept, and Source/VBD/Vcom are kept 0V or floating. 1 : Booster on. (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N will output low during operation.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		B7	B6	B5	B4	B3	B2	B1	B0		B[7] ~ LUT_EN 0: During reset, auto load LUT from MTP if it is valid. When PON/DRF, analog setting will follow the content of MTP. (Default) 1: During reset, no action to load LUT from MTP. When PON/DRF, analog setting will follow the content of MCU B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating) B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating. B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading MTP, Temperature Sensor will be activated automatically one time. (default) B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND. B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																		
0	0	01	0	0	0	0	0	0	0	1	PWR	Power setting Register A[5:0] = 07h [POR] B[7:0] = F0h [POR] C[6:0] = 00h [POR] D[6:0] = 00h [POR] E[6:0] = 00h [POR] F[6:0] = 00h [POR]																		
0	1		0	0	0	0	0	A ₂	A ₁	A ₀		A[2] ~ VSC_EN Source LV power selection: 0: External source power for VSH2 pin. 1: Internal DCDC function for generate source power. (default) A[1] ~ VS_EN Source LV power selection: 0: External source power for VSH1 and VSL pin. 1: Internal DCDC function for generate source power. (default) A[0] ~ VG_EN Gate power selection: 0: External gate power for VGH and VGL pin. 1: Internal DCDC function for generate gate power. (default)																		
0	1		1	1	1	1	0	0	B ₁	B ₀		B[1:0] ~ VGPN [1:0] Internal VGH / VGL Voltage Level Selection: <table><tr><th>VGPN [1:0]</th><th>Gate Voltage Level</th></tr><tr><td>00</td><td>VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V</td></tr><tr><td>01</td><td>VGH=17V ,VGL=-17V VSH=15V, VSL=-15V</td></tr><tr><td>10</td><td>VGH=15V,VGL=-15V VSH=13V, VSL=-13V</td></tr><tr><td>11</td><td>Reserved.</td></tr></table>	VGPN [1:0]	Gate Voltage Level	00	VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V	01	VGH=17V ,VGL=-17V VSH=15V, VSL=-15V	10	VGH=15V,VGL=-15V VSH=13V, VSL=-13V	11	Reserved.								
VGPN [1:0]	Gate Voltage Level																													
00	VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V																													
01	VGH=17V ,VGL=-17V VSH=15V, VSL=-15V																													
10	VGH=15V,VGL=-15V VSH=13V, VSL=-13V																													
11	Reserved.																													
0	1		0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		C[6:0] ~ VSPL [6:0] Internal Source Voltage Level Selection for VSH2@Mode0: <table><tr><th>VSPL[6:0]</th><th>Voltage Level</th></tr><tr><td>00h</td><td>3.0V (default)</td></tr><tr><td>02h</td><td>3.2V</td></tr><tr><td>04h</td><td>3.4V</td></tr><tr><td>06h</td><td>3.6V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>76h</td><td>14.8V</td></tr><tr><td>78h</td><td>15.0V</td></tr><tr><td>Other</td><td>Reserved</td></tr></table>	VSPL[6:0]	Voltage Level	00h	3.0V (default)	02h	3.2V	04h	3.4V	06h	3.6V	:	:	76h	14.8V	78h	15.0V	Other	Reserved
VSPL[6:0]	Voltage Level																													
00h	3.0V (default)																													
02h	3.2V																													
04h	3.4V																													
06h	3.6V																													
:	:																													
76h	14.8V																													
78h	15.0V																													
Other	Reserved																													
0	1		0	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[6:0] ~ VSNL[6:0] Internal Source Voltage Level Selection for VSL@Mode1: <table><tr><th>VSNL[6:0]</th><th>Voltage Level</th></tr><tr><td>00h</td><td>-3.0V (default)</td></tr><tr><td>02h</td><td>-3.2V</td></tr><tr><td>04h</td><td>-3.4V</td></tr><tr><td>06h</td><td>-3.6V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>76h</td><td>-14.8V</td></tr><tr><td>78h</td><td>-15.0V</td></tr><tr><td>Other</td><td>Reserved</td></tr></table>	VSNL[6:0]	Voltage Level	00h	-3.0V (default)	02h	-3.2V	04h	-3.4V	06h	-3.6V	:	:	76h	-14.8V	78h	-15.0V	Other	Reserved
VSNL[6:0]	Voltage Level																													
00h	-3.0V (default)																													
02h	-3.2V																													
04h	-3.4V																													
06h	-3.6V																													
:	:																													
76h	-14.8V																													
78h	-15.0V																													
Other	Reserved																													

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																		
0	1		0	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		E[6:0] ~ VSPL2[6:0] Internal Source Voltage Level Selection for VSH1@Mode1: <table><tr><th>VSPL2[6:0]</th><th>Voltage Level</th></tr><tr><td>00h</td><td>3.0V (default)</td></tr><tr><td>02h</td><td>3.2V</td></tr><tr><td>04h</td><td>3.4V</td></tr><tr><td>06h</td><td>3.6V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>76h</td><td>14.8V</td></tr><tr><td>78h</td><td>15.0V</td></tr><tr><td>Other</td><td>Reserved</td></tr></table>	VSPL2[6:0]	Voltage Level	00h	3.0V (default)	02h	3.2V	04h	3.4V	06h	3.6V	:	:	76h	14.8V	78h	15.0V	Other	Reserved
VSPL2[6:0]	Voltage Level																													
00h	3.0V (default)																													
02h	3.2V																													
04h	3.4V																													
06h	3.6V																													
:	:																													
76h	14.8V																													
78h	15.0V																													
Other	Reserved																													
0	1		0	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀	F[6:0] ~ VSNL2[6:0] Internal Source Voltage Level Selection for VSH2@Mode1: <table><tr><th>VSNL2[6:0]</th><th>Voltage Level</th></tr><tr><td>00h</td><td>3.0V (default)</td></tr><tr><td>02h</td><td>3.2V</td></tr><tr><td>04h</td><td>3.4V</td></tr><tr><td>06h</td><td>3.6V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>76h</td><td>14.8V</td></tr><tr><td>78h</td><td>15.0V</td></tr><tr><td>Other</td><td>Reserved</td></tr></table> VSH1 should be always >= VSH2 Mode0: VSH1=15V, VSL=-15V, VSH2=3~15V Mode1: VSH1=3~15V, VSL=-3~-15V, VSH2=3~15V *Remark: If VGH/VGL <+/- 15V, VSH/VSH2/VSL (max) = (VGH-2V / VGL+2V)	VSNL2[6:0]	Voltage Level	00h	3.0V (default)	02h	3.2V	04h	3.4V	06h	3.6V	:	:	76h	14.8V	78h	15.0V	Other	Reserved	
VSNL2[6:0]	Voltage Level																													
00h	3.0V (default)																													
02h	3.2V																													
04h	3.4V																													
06h	3.6V																													
:	:																													
76h	14.8V																													
78h	15.0V																													
Other	Reserved																													
0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register																		
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence. BUSY_N will output low during operation. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only																		
0	0	03	0	0	0	0	0	0	1	1	POFS	Power on/off Sequence Setting Register A[7:0] = 00h [POR]																		
0	1		0	0	A ₅	A ₄	0	0	A ₁	A ₀		A[5:4] ~ T_VDPG_OFF[1:0] Power off delay from VGL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b: 80ms A[1:0] ~ T_VDS_OFF[1:0] Power off delay from VSHX/VSL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b : 80ms																		

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																				
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register After the Power ON command, driver will power on based on the Power ON Sequence. BUSY_N will output low during operation. * Remark: PON Include booster on, VSHx/VSLx regulator on With default BTST, timing is >80ms																																				
0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register (for VGH) A[6:0] = 0Fh [POR] B[6:0] = 8Bh [POR] C[6:0] = 9Ch [POR] D[6:0] = 96h [POR]																																				
0	1		0	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[6:4] ~ VGHSSC_ONT [2:0] VGH booster maximum MOSFET ON time (reserved) A[6:4] = 000 (Default)																																				
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																						
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																						
0	1		1	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																						
												A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration																																				
												<table><tr><th colspan="4">Soft Start Phase Period (ms)</th></tr><tr><td>00</td><td colspan="3">10</td></tr><tr><td>01</td><td colspan="3">20</td></tr><tr><td>10</td><td colspan="3">30</td></tr><tr><td>11</td><td colspan="3">40</td></tr></table>	Soft Start Phase Period (ms)				00	10			01	20			10	30			11	40																		
Soft Start Phase Period (ms)																																																
00	10																																															
01	20																																															
10	30																																															
11	40																																															
												B[6:4] ~ VGHSSA_DRV [2:0], = 000 (Default) VGH Phase A Driving Strength C[6:4] ~ VGHSSB_DRV [2:0], = 001 (Default) VGH Phase B Driving Strength D[6:4] ~ VGHSSC_DRV [2:0] = 001 (Default) VGH Phase C Driving Strength																																				
												<table><tr><th colspan="4">Driving Strength</th></tr><tr><td>000</td><td>0</td><td>100</td><td>(reserved)</td></tr><tr><td>001</td><td>1</td><td>101</td><td>(reserved)</td></tr><tr><td>010</td><td>2</td><td>110</td><td>(reserved)</td></tr><tr><td>011</td><td>3(strongest)</td><td>111</td><td>(reserved)</td></tr></table>	Driving Strength				000	0	100	(reserved)	001	1	101	(reserved)	010	2	110	(reserved)	011	3(strongest)	111	(reserved)																
Driving Strength																																																
000	0	100	(reserved)																																													
001	1	101	(reserved)																																													
010	2	110	(reserved)																																													
011	3(strongest)	111	(reserved)																																													
												B[3:0] ~ VGHSSA_OFFT [3:0], = 1011 (Default) VGH Phase A Minimum OFF Time C[3:0] ~ VGHSSB_OFFT [3:0], = 1100 (Default) VGH Phase B Minimum OFF Time D[3:0] ~ VGHSSC_OFFT [3:0], = 0110 (Default) VGH Phase C Minimum OFF Time																																				
												<table><tr><th colspan="4">Minimum OFF Time (setting)</th></tr><tr><td>0000</td><td>OFFH0</td><td>1000</td><td>OFFH8</td></tr><tr><td>0001</td><td>OFFH1</td><td>1001</td><td>OFFH9</td></tr><tr><td>0010</td><td>OFFH2</td><td>1010</td><td>OFFHA</td></tr><tr><td>0011</td><td>OFFH3</td><td>1011</td><td>OFFHB</td></tr><tr><td>0100</td><td>OFFH4</td><td>1100</td><td>OFFHC</td></tr><tr><td>0101</td><td>OFFH5</td><td>1101</td><td>OFFHD</td></tr><tr><td>0110</td><td>OFFH6</td><td>1110</td><td>OFFHE</td></tr><tr><td>0111</td><td>OFFH7</td><td>1111</td><td>OFFHF</td></tr></table>	Minimum OFF Time (setting)				0000	OFFH0	1000	OFFH8	0001	OFFH1	1001	OFFH9	0010	OFFH2	1010	OFFHA	0011	OFFH3	1011	OFFHB	0100	OFFH4	1100	OFFHC	0101	OFFH5	1101	OFFHD	0110	OFFH6	1110	OFFHE	0111	OFFH7	1111	OFFHF
Minimum OFF Time (setting)																																																
0000	OFFH0	1000	OFFH8																																													
0001	OFFH1	1001	OFFH9																																													
0010	OFFH2	1010	OFFHA																																													
0011	OFFH3	1011	OFFHB																																													
0100	OFFH4	1100	OFFHC																																													
0101	OFFH5	1101	OFFHD																																													
0110	OFFH6	1110	OFFHE																																													
0111	OFFH7	1111	OFFHF																																													

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description															
0	0	07	0	0	0	0	0	1	1	1	DSLTP	Deep Sleep Register															
0	1		1	0	1	0	0	1	0	1		This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.															
0	0	10	0	0	0	1	0	0	0	0	DTM	Data Start transmission Register															
2 bit per pixel												This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel. KPixel[1:0] Source Driver Output <table><tr><td></td><td>DDX=1 (Default)</td><td>DDX=0</td></tr><tr><td>00b</td><td>Gray 0</td><td>Gray 3</td></tr><tr><td>01b</td><td>Gray 1</td><td>Gray 2</td></tr><tr><td>10b</td><td>Gray 2</td><td>Gray 1</td></tr><tr><td>11b</td><td>Gray 3</td><td>Gray 0</td></tr></table> After issue this command, the host must send at least 1-byte data to the device.		DDX=1 (Default)	DDX=0	00b	Gray 0	Gray 3	01b	Gray 1	Gray 2	10b	Gray 2	Gray 1	11b	Gray 3	Gray 0
	DDX=1 (Default)	DDX=0																									
00b	Gray 0	Gray 3																									
01b	Gray 1	Gray 2																									
10b	Gray 2	Gray 1																									
11b	Gray 3	Gray 0																									
0	1		KPixel1 [1:0]	KPixel2 [1:0]	KPixel3 [1:0]	KPixel4 [1:0]																					
:																											
0	1		KPixel (4M-3) [1:0]	KPixel (4M-2) [1:0]	KPixel (4M-1) [1:0]	KPixel (4M) [1:0]																					
0	0	12	0	0	0	1	0	0	1	0	DRF	Display Refresh Command Register															
0	1		0	0	0	0	0	0	0	0		After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. BUSY_N will output low during operation.															
0	0	17	0	0	0	1	0	1	1	1	AUTO	Auto Sequence Register															
0	1		A7	A6	A5	A4	A3	A2	A1	A0		This command makes the chip enter the auto sequence Single-chip application ONLY. Auto Sequence Option 0xA5: Start Auto Sequence (PON > DRF > POF) 0xA7: Start Auto Sequence (PON > DRF > POF > DSLP). Others: No effect BUSY_N will output low during operation.															

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																					
0	0	30	0	0	1	1	0	0	0	0	PLL	Frame Rate Control register The command controls the clock frequency. A[2:0] = 2h [POR]																					
0	1		0	0	0	0	A ₃	A ₂	A ₁	A ₀		A[3] ~ Dyna Dynamic Frame Rate 0: Disable (Default) 1: Enable A[2:0] ~ FR[2:0] It supports the following frame rates. Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI. <table><tr><th>FR[2:0]</th><th>Frame Rate Selection</th></tr><tr><td>000</td><td>12.5Hz</td></tr><tr><td>001</td><td>25Hz</td></tr><tr><td>010</td><td>50Hz (Default)</td></tr><tr><td>011</td><td>65Hz</td></tr><tr><td>100</td><td>75Hz</td></tr><tr><td>101</td><td>85Hz</td></tr><tr><td>110</td><td>100Hz</td></tr><tr><td>111</td><td>120Hz</td></tr></table>	FR[2:0]	Frame Rate Selection	000	12.5Hz	001	25Hz	010	50Hz (Default)	011	65Hz	100	75Hz	101	85Hz	110	100Hz	111	120Hz			
FR[2:0]	Frame Rate Selection																																
000	12.5Hz																																
001	25Hz																																
010	50Hz (Default)																																
011	65Hz																																
100	75Hz																																
101	85Hz																																
110	100Hz																																
111	120Hz																																
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS [7:0]																					
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		<table><tr><th>TS [7:0]</th><th>Return Value(degC)</th></tr><tr><td>E7h</td><td>-25</td></tr><tr><td>...</td><td>...</td></tr><tr><td>FFh</td><td>-1</td></tr><tr><td>00h</td><td>0</td></tr><tr><td>01h</td><td>1</td></tr><tr><td>...</td><td>...</td></tr><tr><td>19h</td><td>25</td></tr><tr><td>...</td><td>...</td></tr><tr><td>31h</td><td>49</td></tr><tr><td>32h</td><td>50</td></tr></table>	TS [7:0]	Return Value(degC)	E7h	-25	...	...	FFh	-1	00h	0	01h	1	...	...	19h	25	...	...	31h	49	32h
TS [7:0]	Return Value(degC)																																
E7h	-25																																
...	...																																
FFh	-1																																
00h	0																																
01h	1																																
...	...																																
19h	25																																
...	...																																
31h	49																																
32h	50																																
0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register This command selects Temperature offset A[7:0] = 00h [POR]																					
0	1		0	0	0	0	A ₃	A ₂	A ₁	0		A[3:1] ~ TO[3:1] , Temperature offset: <table><tr><th>TO[3:1]</th><th>Calculation</th><th>TO[3:1]</th><th>Calculation</th></tr><tr><td>000</td><td>+0</td><td>100</td><td>-4</td></tr><tr><td>001</td><td>+1</td><td>101</td><td>-3</td></tr><tr><td>010</td><td>+2</td><td>110</td><td>-2</td></tr><tr><td>011</td><td>+3</td><td>111</td><td>-1</td></tr></table>	TO[3:1]	Calculation	TO[3:1]	Calculation	000	+0	100	-4	001	+1	101	-3	010	+2	110	-2	011	+3	111	-1	
TO[3:1]	Calculation	TO[3:1]	Calculation																														
000	+0	100	-4																														
001	+1	101	-3																														
010	+2	110	-2																														
011	+3	111	-1																														

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																								
0	0	50	0	1	0	1	0	0	0	0	CDI	VCOM and DATA interval setting Register This command indicates the Border Output Selection and the interval between Vcom and data output A[7:0] = 97h [POR]																																																								
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:5]~VBD [2:0] Border Output Selection: <table><tr><td></td><td>DDX=1</td><td>DDX=0</td></tr><tr><td>VBD[2:0]</td><td>LUT (Default)</td><td>LUT</td></tr><tr><td>000</td><td>Gray 0</td><td>HIZ</td></tr><tr><td>001</td><td>Gray 1</td><td>Gray 3</td></tr><tr><td>010</td><td>Gray 2</td><td>Gray 2</td></tr><tr><td>011</td><td>Gray 3</td><td>Gray 1</td></tr><tr><td>100</td><td>HIZ(Default)</td><td>Gray 0</td></tr></table> A[4]: DDX Data Polarity for Pixel Data (See DTM command) 0: Invert 1: Non-invert (Default) A[3:0] ~ CDI[3:0] Gate and source blanking time (No gate source scanning) <table><tr><td>CDI [3:0]</td><td>Interval (ms)</td><td>CDI [3:0]</td><td>Interval (ms)</td></tr><tr><td>0h</td><td>2</td><td>8h</td><td>40</td></tr><tr><td>1h</td><td>4</td><td>9h</td><td>60</td></tr><tr><td>2h</td><td>8</td><td>Ah</td><td>80</td></tr><tr><td>3h</td><td>12</td><td>Bh</td><td>100</td></tr><tr><td>4h</td><td>14</td><td>Ch</td><td>120</td></tr><tr><td>5h</td><td>16</td><td>Dh</td><td>140</td></tr><tr><td>6h</td><td>18</td><td>Eh</td><td>160</td></tr><tr><td>7h</td><td>20 (Default)</td><td>Fh</td><td>Reserved</td></tr></table> User needs to review CDI setting to have stable VCOM in application		DDX=1	DDX=0	VBD[2:0]	LUT (Default)	LUT	000	Gray 0	HIZ	001	Gray 1	Gray 3	010	Gray 2	Gray 2	011	Gray 3	Gray 1	100	HIZ(Default)	Gray 0	CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)	0h	2	8h	40	1h	4	9h	60	2h	8	Ah	80	3h	12	Bh	100	4h	14	Ch	120	5h	16	Dh	140	6h	18	Eh	160	7h	20 (Default)	Fh
	DDX=1	DDX=0																																																																		
VBD[2:0]	LUT (Default)	LUT																																																																		
000	Gray 0	HIZ																																																																		
001	Gray 1	Gray 3																																																																		
010	Gray 2	Gray 2																																																																		
011	Gray 3	Gray 1																																																																		
100	HIZ(Default)	Gray 0																																																																		
CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)																																																																	
0h	2	8h	40																																																																	
1h	4	9h	60																																																																	
2h	8	Ah	80																																																																	
3h	12	Bh	100																																																																	
4h	14	Ch	120																																																																	
5h	16	Dh	140																																																																	
6h	18	Eh	160																																																																	
7h	20 (Default)	Fh	Reserved																																																																	
0	0	51	0	1	0	1	0	0	0	1	LPD	Lower Power Detection Register																																																								
1	1		0	0	0	0	0	0	0	A ₀		BUSY_N will output low during operation. Then the LPD status can be read. A[0] ~ LPD status 0: Low power input VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL 1: Normal (default)																																																								
0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register A[7:0] = C8h [POR] B[7:0] = C8h [POR]																																																								
0	1		0	0	0	0	0	0	0	0		This command defines alternative resolution A[7:0] ~ HRES[7:0] Horizontal Display Resolution Remark: Horizontal resolution should be 4-multiple.																																																								
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[7:0] ~ VRES[7:0] Vertical Display Resolution e.g. HRES= C8h, VRES= C8h																																																								
0	1		0	0	0	0	0	0	0	0		<table><tr><td>UD,SHL</td><td>Source and gate sequence</td></tr><tr><td>00</td><td>S199,G199 to S0,G0</td></tr><tr><td>01</td><td>S0, G199 to S199,G0</td></tr><tr><td>10</td><td>S199,G0 to S0, G199</td></tr><tr><td>11</td><td>S0,G0 to S199, G199</td></tr></table>	UD,SHL	Source and gate sequence	00	S199,G199 to S0,G0	01	S0, G199 to S199,G0	10	S199,G0 to S0, G199	11	S0,G0 to S199, G199																																														
UD,SHL	Source and gate sequence																																																																			
00	S199,G199 to S0,G0																																																																			
01	S0, G199 to S199,G0																																																																			
10	S199,G0 to S0, G199																																																																			
11	S0,G0 to S199, G199																																																																			
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	Remark: 1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command. 2) VRES[7:0] >= 79																																																									

SSD2681 products shall only be used solely with Permitted E5 Spectra 3100 FPL licensed by E Ink, customer should notify the same acknowledgement with its downstream customers.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																
0	0	62	0	1	1	0	0	0	1	0	HTOTAL	HTOTAL setting Register. This command defines line time for different frame rate. A[7:0] = 0x64 [POR], B[7:0] = 0x53 [POR]																
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		Which defined the line time for HTOTAL_A to HTOTAL_B respectively. Frame time = HTOTAL timing x TRES.VRES[7:0] Timing of POR is matched for VRES = 200. Remark: 1) HTOTAL is effective when PSR.RES=2'b00 2) If user used TRES to define resolution, it needs to set the corresponding HTOTAL. Please refer to application note for details setting.																
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																		
0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register. A[7:0] = 00h [POR] B[7:0] = 00h [POR]																
0	1		0	0	0	0	0	0	0	0		A[7:0] ~ S_start[7:0] First valid source output channel setting <table><tr><th>S_start [7:0]</th><th>First valid source output</th></tr><tr><td>00h</td><td>S0 (Default)</td></tr><tr><td>04h</td><td>S4</td></tr><tr><td>08h</td><td>S8</td></tr><tr><td>...</td><td>...</td></tr><tr><td>C0h</td><td>S192</td></tr><tr><td>C4h</td><td>S196</td></tr><tr><td>Other</td><td>Reserved</td></tr></table>	S_start [7:0]	First valid source output	00h	S0 (Default)	04h	S4	08h	S8	...	...	C0h	S192	C4h	S196	Other	Reserved
S_start [7:0]	First valid source output																											
00h	S0 (Default)																											
04h	S4																											
08h	S8																											
...	...																											
C0h	S192																											
C4h	S196																											
Other	Reserved																											
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																		
0	1		0	0	0	0	0	0	0	0																		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																		
												B[7:0] ~ G_start[7:0] First valid gate output channel setting GSST and TRES can define the display window from target source and gate start and end line. GD: First G active = G16, G_start[7:0]=16. Last G active = G175, VRES[7:0]=160. SD: First S active = S8, S_start[7:0]=8. Last S active = S119, HRES[7:0]=112. Remark: 1) PSR.RES[1:0] = 00 2) G_start+VRES< 200, S_start+HRES< 200.																
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0] = 48h [POR] B[7:0] = 01h [POR] C[7:0] = 01h [POR]																
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																		
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																		
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																	
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]																	
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	0	A ₀		A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16 A[5:4] ~AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec. A[3] ~ AMVX VCOM measurement Gate settings 0: Gate scan normally during VCOM measurement (Default) 1: All Gates ON during VCOM measurement A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (Default) 1: Set Source output to VSH_LV during Auto Measure VCOM period. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled BUSY_N will output low during operation. Requirement: AMV works at PON only																	
0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.																	
1	1		1	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[5:0] ~ VV[5:0]: Vcom read Value, valid range from -0.2V to -3.0V. <table><tr><th>VV[5:0]</th><th>Vcom read value</th></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>...</td><td>...</td></tr><tr><td>3Ch</td><td>-3.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table>	VV[5:0]	Vcom read value	00h	Reserved	04h	-0.2V	08h	-0.4V	0Ch	-0.6V	10h	-0.8V	...	...	3Ch	-3.0V	others
VV[5:0]	Vcom read value																												
00h	Reserved																												
04h	-0.2V																												
08h	-0.4V																												
0Ch	-0.6V																												
10h	-0.8V																												
...	...																												
3Ch	-3.0V																												
others	Reserved																												

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																		
0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]																		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	0	0		A[7] ~ MTP_VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from MTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.2V step from -0.2V to -3V. <table><tr><th>VDCS [6:0]</th><th>VCOM_DC Setting</th></tr><tr><td>00h</td><td>Reserved</td></tr><tr><td>04h</td><td>-0.2V</td></tr><tr><td>08h</td><td>-0.4V</td></tr><tr><td>0Ch</td><td>-0.6V</td></tr><tr><td>10h</td><td>-0.8V</td></tr><tr><td>...</td><td>...</td></tr><tr><td>3Ch</td><td>-3.0V</td></tr><tr><td>others</td><td>Reserved</td></tr></table>	VDCS [6:0]	VCOM_DC Setting	00h	Reserved	04h	-0.2V	08h	-0.4V	0Ch	-0.6V	10h	-0.8V	...	...	3Ch	-3.0V	others	Reserved
VDCS [6:0]	VCOM_DC Setting																													
00h	Reserved																													
04h	-0.2V																													
08h	-0.4V																													
0Ch	-0.6V																													
10h	-0.8V																													
...	...																													
3Ch	-3.0V																													
others	Reserved																													
0	0	83	1	0	0	0	0	0	1	1	PTLW	PARTIAL WINDOW This command sets partial window address. A[7:0] = 00h [POR] B[7:0] = C7h [POR] C[7:0] = 00h [POR] D[7:0] = C7h [POR] E[7:0] = 00h [POR]																		
0	1		0	0	0	0	0	0	0	0		A[7:0] ~ HRST [7:0] Horizontal start address																		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[7:0] ~ HRED [7:0] Horizontal end address																		
0	1		0	0	0	0	0	0	0	0		C[7:0] ~ VRST [7:0] Vertical start address																		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		D[7:0] ~ VRED [7:0] Vertical end address																		
0	1		0	0	0	0	0	0	0	0		E[0] ~ PMODE 0: disable partial mode (Default) 1: enable partial mode Gate scan both inside and outside of the partial window																		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		Note: 1) HRST [7:0]<= HRED [7:0] 2) VRST [7:0]<= VRED [7:0]																		
0	1		0	0	0	0	0	0	0	0																				
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																				
0	1		0	0	0	0	0	0	0	E ₀																				
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set MTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode BUSY_N will output low until PGM mode is ready.																		
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to execute MTP program After this command is issued, the chip would program the MTP. BUSY_N will output low during operation. Requirement: In PON mode with internal programming power.																		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	92	1	0	0	1	0	0	1	0	RMTP	Read MTP Data
1	1		1 st ~ dummy 2 nd ~ N+1th Parameter									This command is to read the MTP content from SRAM. The 1 st byte read is dummy byte. The 2 nd byte read is the content of Address 0 in MTP The N+1 th byte read is the content of Address n in MTP After issue this command, the host must read at least 1 byte data from the device.
0	0	A2	1	0	1	0	0	0	1	0	PGM_CFG	MTP Program Config
0	1		0	0	0	0	0	0	A1	A0		This command is to set the configuration of MTP.
0	1		B7	B6	B5	B4	B3	B2	B1	B0		A[1:0] ~ PGM_UMODE[1:0] 00: Reserved
0	1		C7	C6	C5	C4	C3	C2	C1	C0		01: Compressed LUT (Default) 10: Init code 11: Raw mode
0	1		D7	D6	D5	D4	D3	D2	D1	D0		B[7:0] ~ PGM_SADDR[15:8], C[7:0] ~ PGM_SADDR[7:0]
0	1		E7	E6	E5	E4	E3	E2	E1	E0		Program Start Address: Compressed LUT: 0000h D[7:0] ~ PGM_DSIZE [15:8] E[7:0] ~ PGM_DSIZE [7:0] Program Data Size: Compressed LUT: Size in bytes
0	0	A3	1	0	1	0	0	0	1	1	PGM_STAT	MTP Program Status
1	1		0	0	0	0	0	0	A1	A0		This command is to read MTP Program status A[7:0] = 00h [POR] A[1] ~ PGM_VER_ERR Data verification of APG 0: OK 1: NOK A[0] ~ PGM_EXE_ERR MTP program execution status 0: Normal 1: Invalid APG setting
0	0	A4	1	0	1	0	0	1	0	0	MTP_STAT	MTP Status Register
1	1		0	0	0	0	0	0	A1	A0		This command is to read MTP status A[7:0] = 00h [POR] B[7:0] = 00h [POR] C[7:0] = 00h [POR]
1	1		0	0	0	0	0	0	A1	A0		A[1:0] :LUT Type
1	1		0	0	0	0	B3	B2	B1	B0		User MTP Type
1	1		C7	C6	C5	C4	C3	C2	C1	C0		0: Blank 1: Compressed Others: ~ Reserved B[3:0] ~ FREE_BLK[3:0] Next Free compressed data block number. C[7:0] ~ FREE_UI[7:0] Next Free Space Address for User Init Code

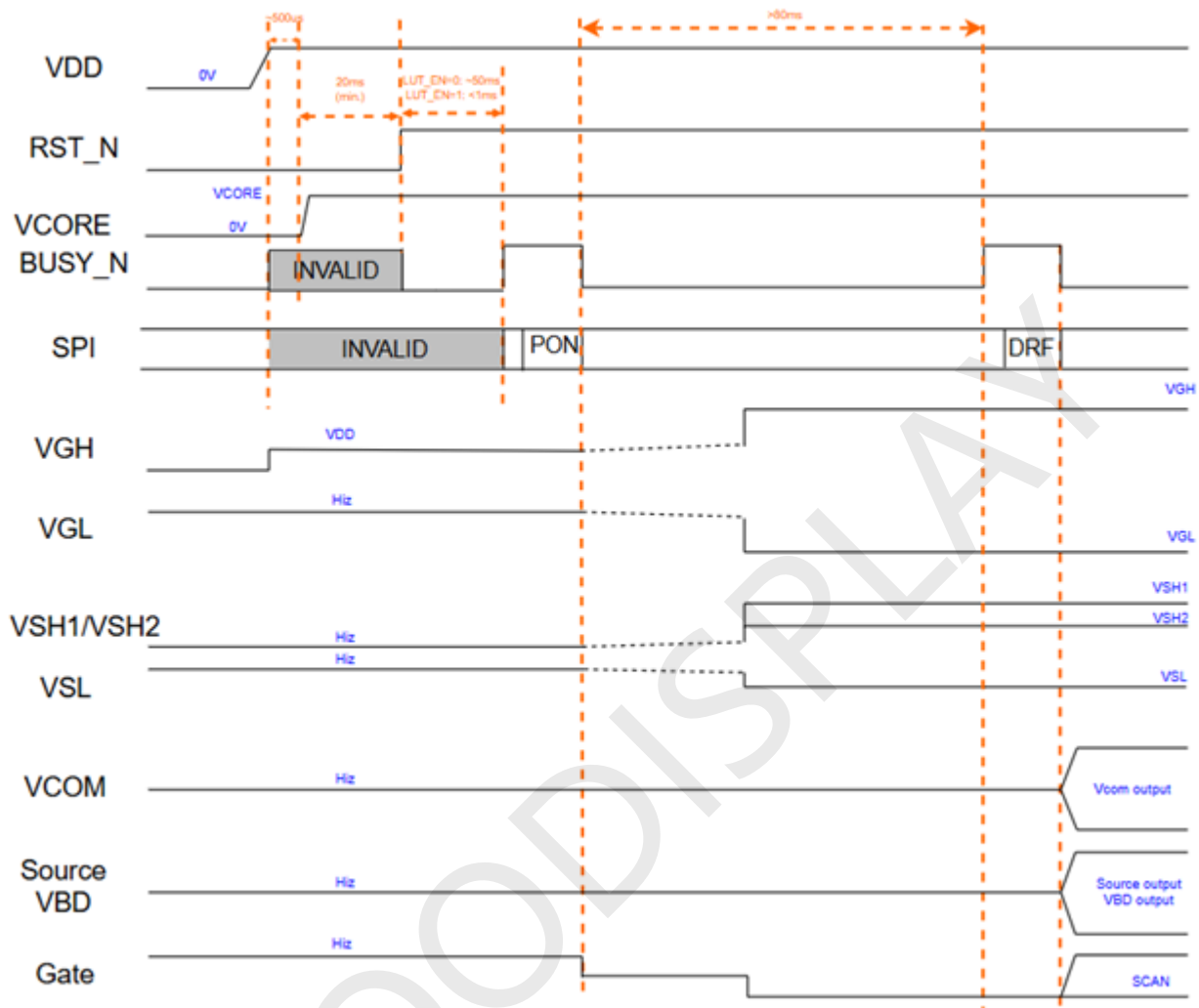
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																							
0	0	E0	1	1	1	0	0	0	0	0	CCSET	CCSET for temperature input selection A[7:0] = 00h [POR]																																																																							
0	1		0	0	0	0	0	0	A ₁	0		A[1] = TSFIX Temperature Input selection 0: Use Internal Temperature sensor (Default) 1: Use TSSET[7:0] value																																																																							
0	0	E3	1	1	1	0	0	0	1	1	PWS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]																																																																							
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. A[7:4] = VCOM_W [3:0] <table><tr><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th></tr><tr><td>0</td><td>Reserved</td><td>8</td><td>8</td></tr><tr><td>1</td><td>1</td><td>9</td><td>9</td></tr><tr><td>2</td><td>2</td><td>10</td><td>10</td></tr><tr><td>3</td><td>3</td><td>11</td><td>11</td></tr><tr><td>4</td><td>4</td><td>12</td><td>12</td></tr><tr><td>5</td><td>5</td><td>13</td><td>13</td></tr><tr><td>6</td><td>6 [Default]</td><td>14</td><td>14</td></tr><tr><td>7</td><td>7</td><td>15</td><td>15</td></tr></table> A[3:0] = SD_W [3:0] <table><tr><th>SD_W [3:0]</th><th>Source power saving width[us]</th><th>SD_W [3:0]</th><th>Source power saving width [us]</th></tr><tr><td>0</td><td>Reserved</td><td>8</td><td>4</td></tr><tr><td>1</td><td>0.5</td><td>9</td><td>4.5</td></tr><tr><td>2</td><td>1</td><td>10</td><td>5</td></tr><tr><td>3</td><td>1.5</td><td>11</td><td>5.5</td></tr><tr><td>4</td><td>2</td><td>12</td><td>6</td></tr><tr><td>5</td><td>2.5[Default]</td><td>13</td><td>6.5</td></tr><tr><td>6</td><td>3</td><td>14</td><td>7</td></tr><tr><td>7</td><td>3.5</td><td>15</td><td>7.5</td></tr></table> Remark: VCOM_W setting < CDI setting SD_W setting < S2G setting	VCOM_W [3:0]	VCOM_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)	0	Reserved	8	8	1	1	9	9	2	2	10	10	3	3	11	11	4	4	12	12	5	5	13	13	6	6 [Default]	14	14	7	7	15	15	SD_W [3:0]	Source power saving width[us]	SD_W [3:0]	Source power saving width [us]	0	Reserved	8	4	1	0.5	9	4.5	2	1	10	5	3	1.5	11	5.5	4	2	12	6	5	2.5[Default]	13	6.5	6	3	14	7	7	3.5	15
VCOM_W [3:0]	VCOM_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)																																																																																
0	Reserved	8	8																																																																																
1	1	9	9																																																																																
2	2	10	10																																																																																
3	3	11	11																																																																																
4	4	12	12																																																																																
5	5	13	13																																																																																
6	6 [Default]	14	14																																																																																
7	7	15	15																																																																																
SD_W [3:0]	Source power saving width[us]	SD_W [3:0]	Source power saving width [us]																																																																																
0	Reserved	8	4																																																																																
1	0.5	9	4.5																																																																																
2	1	10	5																																																																																
3	1.5	11	5.5																																																																																
4	2	12	6																																																																																
5	2.5[Default]	13	6.5																																																																																
6	3	14	7																																																																																
7	3.5	15	7.5																																																																																
0	0	E4	1	1	1	0	0	1	0	0	LVSEL	LVD Voltage Select Register This command is sets for low power detect level power A[1:0] = 3h [POR]																																																																							
0	1		0	0	0	0	0	0	A ₁	A ₀		A[1:0] ~ LVD_SEL[1:0] Low power detection threshold 00: 2.2V 01: 2.3V 10: 2.4V 11 : 2.5V (Default)																																																																							

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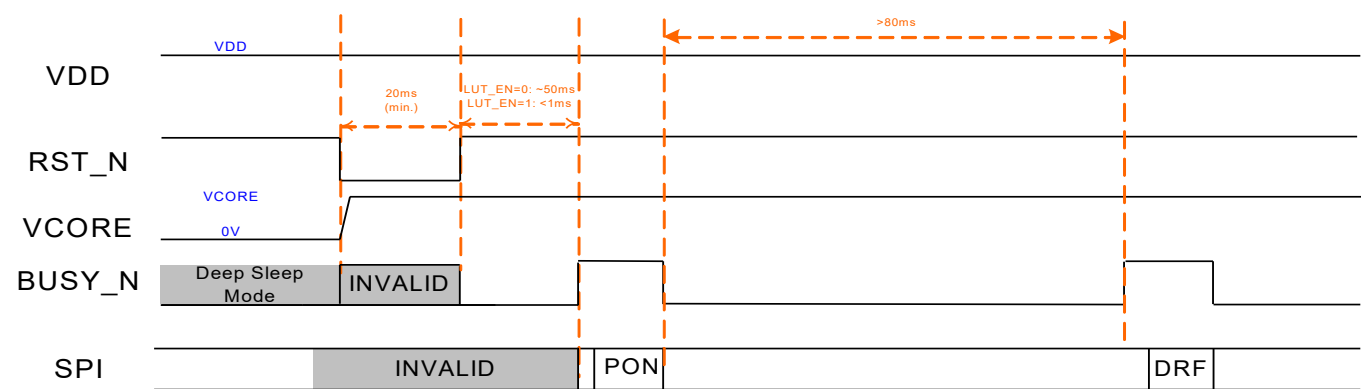
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																							
0	0	E6	1	1	1	0	0	1	1	0	TSSET	Manual input temperature value This command is to force the TS value A[7:0] = 00h [POR]																																																							
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0] ~ TS_SET[7:0] When TSFIX=1, Temperature value will be set by TS_SET[7:0]. Format of the temperature value is 8-bit binary value and it is 1degC per step. <table><tr><th>TS_SET[7:0]</th><th>Force the TS Value(degC)</th></tr><tr><td>E7h</td><td>-25</td></tr><tr><td>...</td><td>...</td></tr><tr><td>FFh</td><td>-1</td></tr><tr><td>00h</td><td>0</td></tr><tr><td>01h</td><td>1</td></tr><tr><td>...</td><td>...</td></tr><tr><td>19h</td><td>25</td></tr><tr><td>...</td><td>...</td></tr><tr><td>31h</td><td>49</td></tr><tr><td>32h</td><td>50</td></tr></table>	TS_SET[7:0]	Force the TS Value(degC)	E7h	-25	...	...	FFh	-1	00h	0	01h	1	...	...	19h	25	...	...	31h	49	32h	50																																	
TS_SET[7:0]	Force the TS Value(degC)																																																																		
E7h	-25																																																																		
...	...																																																																		
FFh	-1																																																																		
00h	0																																																																		
01h	1																																																																		
...	...																																																																		
19h	25																																																																		
...	...																																																																		
31h	49																																																																		
32h	50																																																																		
0	0	E7	1	1	1	0	0	1	1	1	PST	VGH Booster Soft Start Setting Register (for VGH) during switch mode A[6:0] = 16h [POR]																																																							
0	1		0	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[6:4] ~ VGHSM_DRV [2:0], = 001 VGH switch mode Driving Strength <table><tr><th colspan="4">Driving Strength</th></tr><tr><td>000</td><td>0</td><td>100</td><td>(reserved)</td></tr><tr><td>001</td><td>1</td><td>101</td><td>(reserved)</td></tr><tr><td>010</td><td>2</td><td>110</td><td>(reserved)</td></tr><tr><td>011</td><td>3(strongest)</td><td>111</td><td>(reserved)</td></tr></table> A[3:0] ~ VGHSM_OFFT[[3:0], = 0110 VGH switch mode Minimum OFF Time <table><tr><th colspan="4">Minimum OFF Time (setting)</th></tr><tr><td>0000</td><td>OFFH0</td><td>1000</td><td>OFFH8</td></tr><tr><td>0001</td><td>OFFH1</td><td>1001</td><td>OFFH9</td></tr><tr><td>0010</td><td>OFFH2</td><td>1010</td><td>OFFHA</td></tr><tr><td>0011</td><td>OFFH3</td><td>1011</td><td>OFFHB</td></tr><tr><td>0100</td><td>OFFH4</td><td>1100</td><td>OFFHC</td></tr><tr><td>0101</td><td>OFFH5</td><td>1101</td><td>OFFHD</td></tr><tr><td>0110</td><td>OFFH6</td><td>1110</td><td>OFFHE</td></tr><tr><td>0111</td><td>OFFH7</td><td>1111</td><td>OFFHF</td></tr></table> Remark: PSR.B_mode=1	Driving Strength				000	0	100	(reserved)	001	1	101	(reserved)	010	2	110	(reserved)	011	3(strongest)	111	(reserved)	Minimum OFF Time (setting)				0000	OFFH0	1000	OFFH8	0001	OFFH1	1001	OFFH9	0010	OFFH2	1010	OFFHA	0011	OFFH3	1011	OFFHB	0100	OFFH4	1100	OFFHC	0101	OFFH5	1101	OFFHD	0110	OFFH6	1110	OFFHE	0111	OFFH7	1111
Driving Strength																																																																			
000	0	100	(reserved)																																																																
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0001	OFFH1	1001	OFFH9																																																																
0010	OFFH2	1010	OFFHA																																																																
0011	OFFH3	1011	OFFHB																																																																
0100	OFFH4	1100	OFFHC																																																																
0101	OFFH5	1101	OFFHD																																																																
0110	OFFH6	1110	OFFHE																																																																
0111	OFFH7	1111	OFFHF																																																																

9 Display on/off Sequence

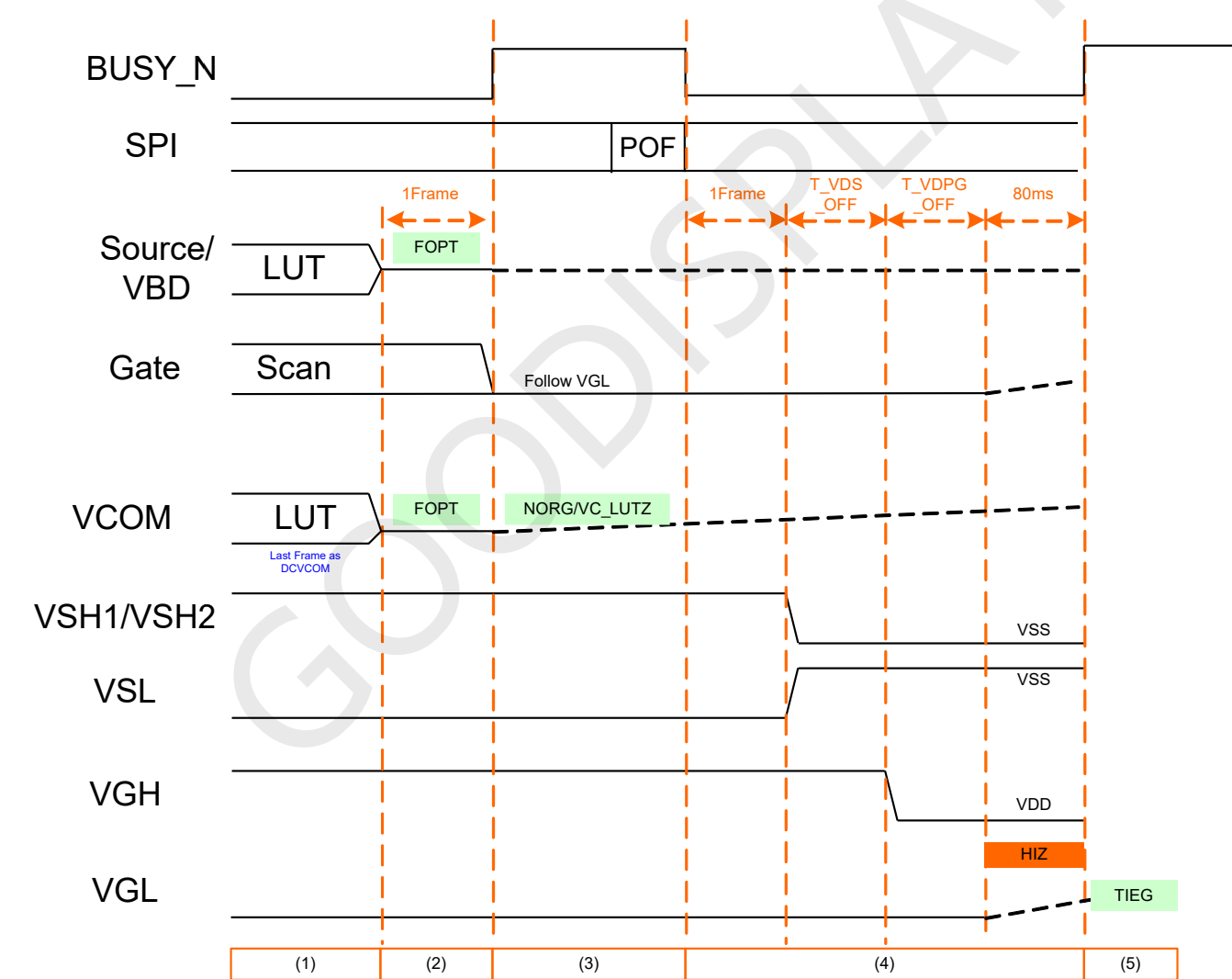
9.1 Display on sequence from VDD power on



9.2 Display on sequence from deep sleep mode



9.3 Display off Sequence Display



Note: If VCOM and VGL set as floating after display update. Please wait until the system completely discharge before next operation.

10 Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V _{DD}	Logic supply voltage	-0.5 to +4.0	V
V _{IN}	Logic Input voltage	-0.5 to V _{DDIO} +0.5	V
V _{OUT}	Logic Output voltage	-0.5 to V _{DDIO} +0.5	V
T _{OPR}	Operation temperature range	-30 to +85	°C
T _{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VDD be constrained to the range GND < VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, T_{OPR}=25°C.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V _{DD}	VDD supply operation voltage	VDD		2.2	3.0	3.6	V
V _{COM_DC}	VCOM_DC output voltage	VCOM		-3.0	-	-0.2	V
dV _{COM_DC}	VCOM_DC output voltage deviation	VCOM	No output load	-200	-	200	mV
V _{COM_AC}	VCOM_AC output voltage	VCOM		V _{SL}	V _{COM_DC}	V _{SH}	V
V _{GATE}	Gate output voltage	G0~G199		-20	-	+20	V
V _{GATE(p-p)}	Gate output peak to peak voltage	G0~G199		-	-	40	V
V _{SH}	Positive Source output voltage	VSH1		+3		+15	V
V _{SH2}	Positive Source output voltage	VSH2		+3		+15	V
dV _{SH}	VSH1/VSH2 output voltage deviation	VSH1/ VSH2	No output load	-200	-	200	mV
V _{SL}	Negative Source output voltage	VSL		-15		-3	V
dV _{SL}	VSL output voltage deviation	VSL	No output load	-200	-	200	mV
V _{IH}	High level input voltage	SDA SCL, CSB, DC, RST_N, BS1		0.8V _{DDIO}	-	-	V
V _{IL}	Low level input voltage			-	-	0.2V _{DDIO}	V
V _{OH}	High level output voltage	SDA, BUSY_N	IOH = -100uA	0.8V _{DDIO}	-	-	V
V _{OL}	Low level output voltage		IOL = 100uA	-	-	0.2V _{DDIO}	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Islp_VDD	Sleep mode current	VDD	- DC/DC off - No clock - No output load - MCU interface access - RAM data access	-	-	35	uA
Idslp_VDD	deep sleep current	VDD	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data	-	-	1	uA
Iopr_VDD	Operating Mode current	VDD	VDD=3V	-	2	-	mA
V _{GH}	Operating Mode Output Voltage	VGH	After PON Command	19.0	20	21.0	V
V _{SH}		VSH1	VGH=20V VGL=-VGH VSH=15V	14.8	15	15.2	V
V _{SH2}		VSH2	VSH2=15V VSL=-15V	14.8	15	15.2	V
V _{SL}		VSL	VCOM = -2V No waveform transitions.	-15.2	-15	-14.8	V
V _{COM}		VCOM	No output load No RAM read/write	-2.2	-2	-1.8	V

12 AC Characteristics

12.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, T_{OPR} = 25°C, CL=20pF

Table 12-1 : Serial Peripheral Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t _{CSS}	CSB select setup time	60			ns
t _{SCH}	CSB select hold time	65			ns
t _{SCC}	CSB deselect setup time	25			ns
t _{CHW}	CSB deselect hold time	100			ns
t _{SCYCW}	Serial clock cycle (Write)	50			ns
t _{SHW}	SCL "H" pulse width (Write)	25			ns
t _{SLW}	SCL "L" pulse width (Write)	25			ns
t _{SCYCL}	Serial clock cycle (Read)	400			ns
t _{SHR}	SCL "H" pulse width (Read)	180			ns
t _{SLR}	SCL "L" pulse width (Read)	180			ns
t _{SDS}	Data setup time	30			ns
t _{SDH}	Data hold time	30			ns
t _{DCS}	DC setup time	40			ns
t _{DCH}	DC hold time	40			ns
t _{ACC}	Access time			100	ns
t _{OH}	Output disable time	15			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

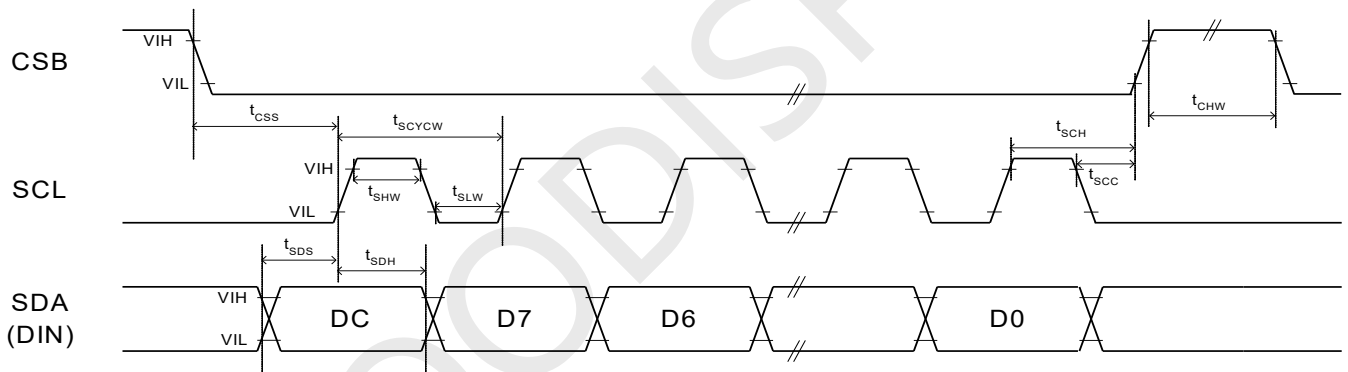


Figure 12-1: 3-wire SPI characteristics (write mode)

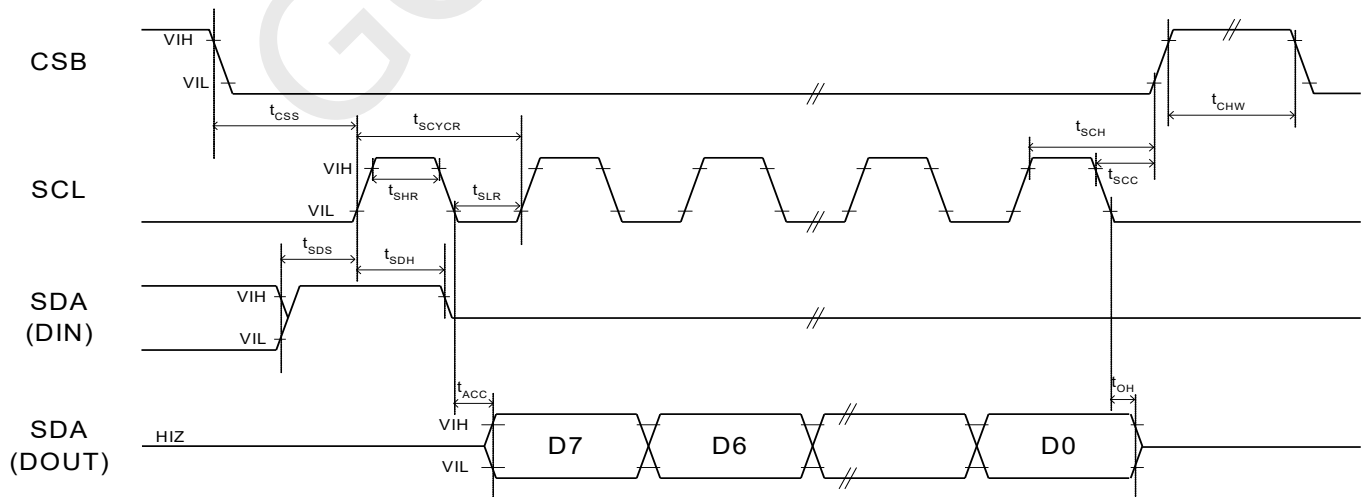


Figure 12-2: 3-wire SPI characteristics (read mode)

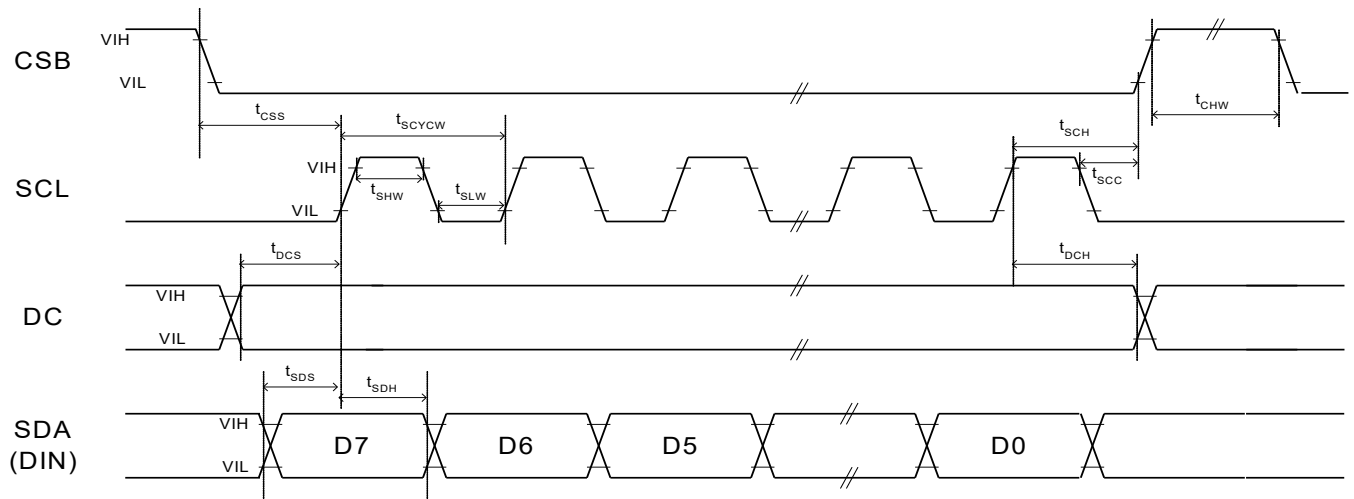


Figure 12-3: 4-wire SPI characteristics (write mode)

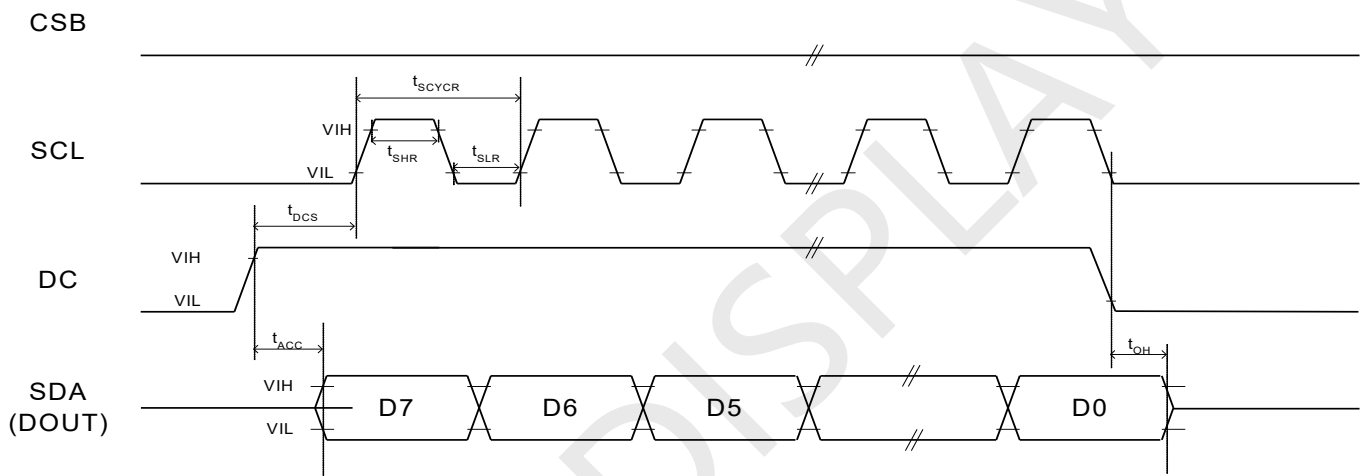


Figure 12-4: 4-wire SPI characteristics (read mode)

13 Application Circuit

Figure 13-1: SSD2681 application circuit

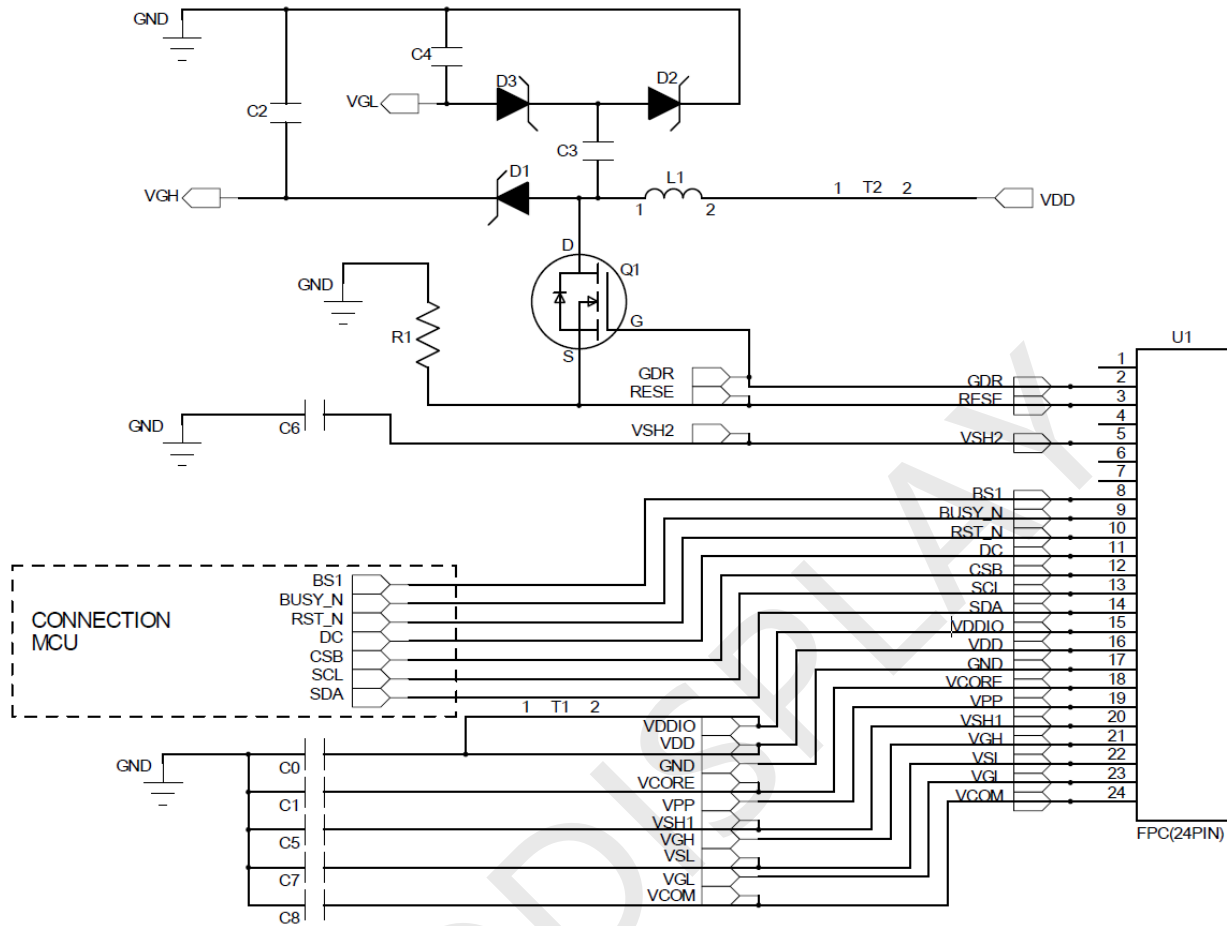


Table 13-1: Component list for SSD2681 application circuit

Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	0.47uF, 1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, $\geq 0.05W$
D1-D3	Diode	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) $I_o \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs(th)} = 0.9V$ (Typ), 1.3V (Max) 3) $R_{ds\ on} \leq 2.1\Omega$ @ $V_{gs} = 2.5V$
L1	47uH	CDRH2D18 / LDNP-470NC $I_o = 500mA$ (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

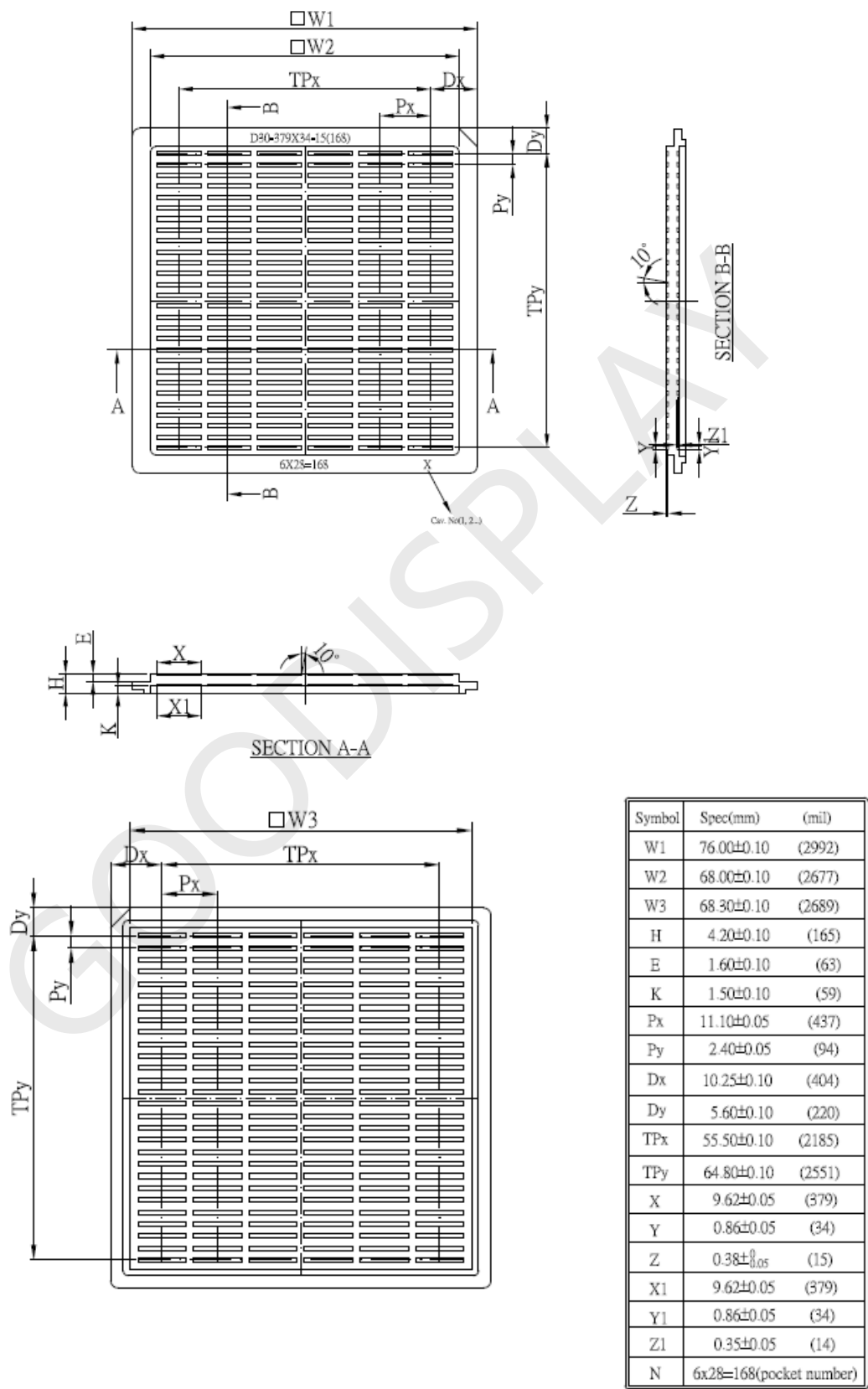
Remarks:

- 1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
- 2) Customer is required to review if the selected component value and part is suitable for their application.

14 Package Information

14.1 Die Tray Dimensions for SSD2681Z2 / SSD2681ZA

Figure 14-1: SSD2681Z2 / SSD2681ZA die tray information (unit: mm)



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