SSD2683

Product Proposal

400 Source x 300 Gate
Active Matrix EPD Display Driver with Controller
for color application

SOLOMON SYSTECH

Appendix: Revision history

Revision	Description of any change	Effective
SSD2683 Product Proposal 0.10	Initial release of product proposal 0.10	23-Apr-2024
SSD2683 Product Proposal 0.20	Updated Feature: “Embedded 3840 Bytes MTP to store the waveform settings and parameters”	16-May-2024

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FIGURES

1 General Description

The SSD2683 is an all-in-one AMEPD driver IC with Controller which can support EPD color application.

It consists of 400 source outputs, 300 gate outputs, 1 VCOM & 1 VBD which can support a maximum display resolution 400 x 300. SSD2683 supports cascade function which can expands the panel resolution to maximum 800x300.

SSD2683 embeds oscillator, booster & regulators and selectable Serial Peripheral Interface (3-wire/4-wire) to communicate with general MCU.

2 Features

- Design for dot matrix type active matrix EPD display, support Black/White/Color
- Power supply:
  - VDD: 2.3V to 3.6V
  - VDDIO: Connect to VDD
- On chip display RAM
  - 2bit outputs per pixel to support Black/White/Color
- Resolution: 400 gate outputs, 300 source outputs, 1 VBD (for border) and 1 VCOM
  - 400 output gate drivers:
    - 2-level outputs (VGH, VGL), Max 40Vp-p
    - Gate driving output voltage (VGH/VGL): +/-20V, +/-17V, +/-15V
    - Up and Down shift capability
  - 300 output source drivers with 4 levels output for black/white/color per pixel:
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame):
      - Mode 0: 0V & VSH1 (+15V) & VSL (-15V) & VSH2 (+3V to +15V)
      - Mode 1: 0V & VSH1 (+3V to +15V) & VSL (-3V to -15V) & VSH2 (+3V to +15V)
    - Source driving output voltage (Voltage step: 200mV)
    - Left and Right shift capability
  - 1 VBD for border level
    - Same function as the programmable source driver with selected LUT
    - 4 levels output (DCVCOM, VSH1, VSL and VSH2)
  - 1 VCOM for Common electrode level
    - DCVCOM: -0.2V to -3V (Voltage step: 200mV)
    - ACVCOM: 4 levels output (DCVCOM, VSH1+DCVCOM, VSL+DCVCOM and floating)
    - Built in VCOM sensing
- On-chip oscillator
- Programmable output Waveform Settings
- Support frame rate: 120Hz (max)
- Embedded 3840 Bytes MTP to store the waveform settings and parameters
- Support low voltage detect for supply voltage
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC, 7-bit status
- MCU interface: Serial peripheral (3-wire/4-wire), Maximum SPI write speed 20MHz
- Available in COG package

3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form	Remark
SSD2683Z2	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 9um
SSD2683ZA	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 9um

4 Block Diagram

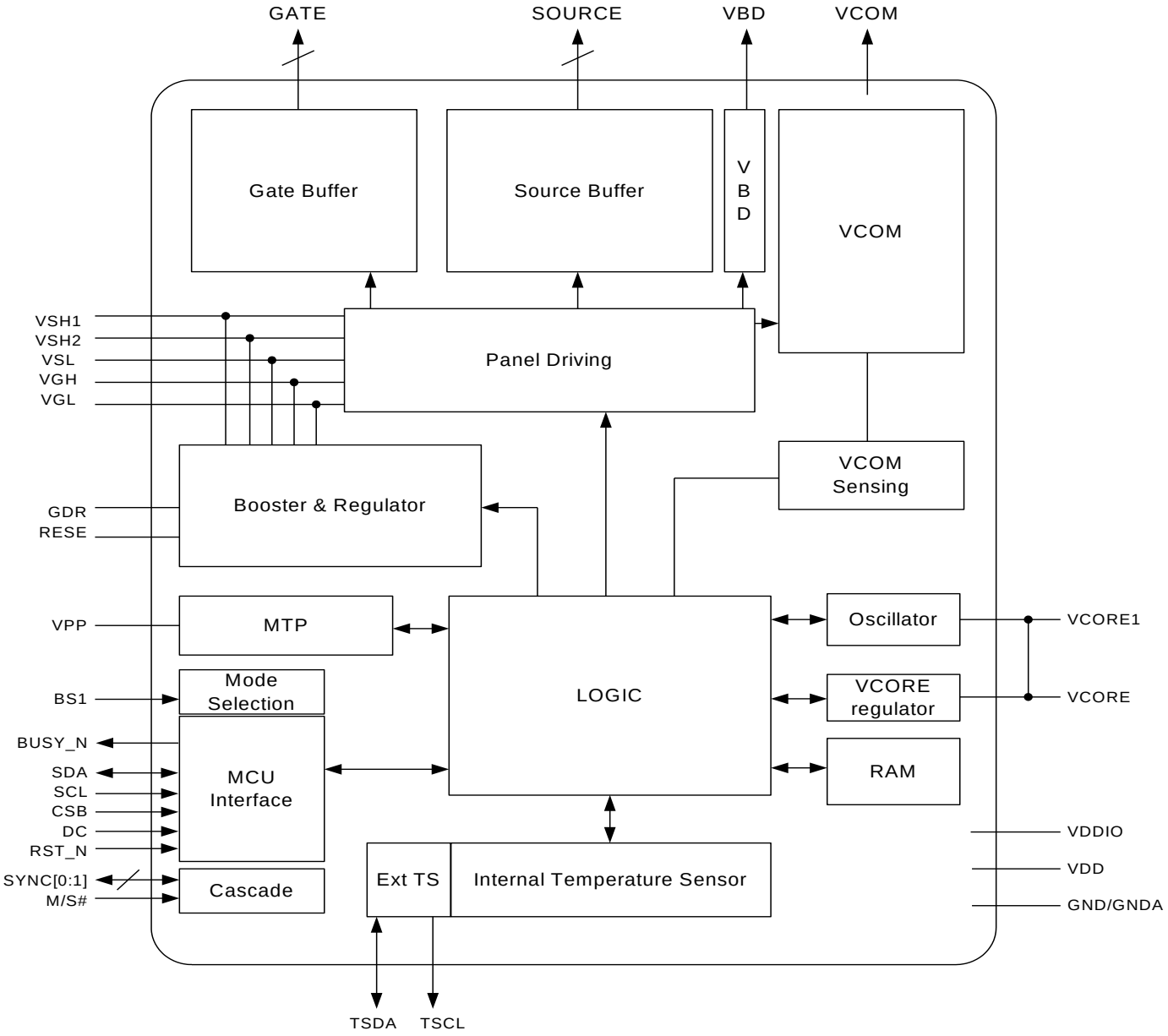


Figure 4-1: SSD2683 Block Diagram

5 PIN DESCRIPTION

Key: I = Input, O = Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L = connect to GND, Pull H = connect to V_{DDIO}

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VDD	P	Power Supply	Power Supply	Power input pin for the chip.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the interface. - Connect to VDD in the application circuit.	-
VCORE	C	Capacitor	Logic Power	Core logic power pin. VCORE is regulated internally from VDD.	-
VCORE1	C	Capacitor	Logic Power	Core logic power pin1. - connect to VCORE in the application circuit	-
GND	P	GND	GND	Ground	-
GNDA	P	GND	GND	Ground - Connect to GND in the application circuit	-
VPP	P	Reserved	Reserved	Reserved Keep it floating.	-

Table 5-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
BS1	I	VDDIO/GND	MCU Interface Mode Selection	This pin is for selecting 3-wire or 4-wire SPI bus. BS1: 0 = 4-wire SPI; 1 = 3-wire SPI(9 bits SPI)	-
SCL	I	MPU	Data Bus	Serial clock pin for interface	-
SDA	I/O	MPU	Data Bus	Serial data pin for interface	-
CSB	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU.	-
DC	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU.	VDDIO or GND
RST_N	I	MPU	System Reset	This pin is reset signal input. Active Low.	-
BUSY_N	O	MPU	Device Busy Signal	This pin indicates the driver status. L: Driver is busy H: non-busy. Host side can send command/data to driver. In the cascade mode, the BUSY_N pin of the slave chip should be left open.	Open

Name	Type	Connect to	Function	Description	When not in use
M/S#	I	VDDIO/GND	Cascade Mode Selection	This pin is Master and Slave selection pin. - For the single chip application, the M/S# pin should be connected to VDDIO. - In the cascade mode: • For Master Chip, the M/S# pin should be connected to VDDIO. • For Slave Chip, the M/S# pin should be connected to GND. The oscillator, booster and regulator circuits of the slave chip will be disabled. The corresponding pins including TSDA, TSCL, SYNC[0:1], VCORE, VGH, VGL, VSH1, VSL, VSH2 VCOM must be connected to the master chip.	-
SYNC[1:0]	I/O	Cascade connection	Cascade application	The corresponding pins must be connected to the master chip for cascade application.	Open
TSDA	I/O	Temperature sensor SDA	Interface to Digital Temp. Sensor	This pin is I^2C Interface to digital temperature sensor Data pin. External pull up resistor is required when using in cascade application or connecting to I^2C slave. The corresponding pins must be connected to the master chip for cascade application.	GND
TSCL	O	Temperature sensor SCL	Interface to Digital Temp. Sensor	This pin is I^2C Interface to digital temperature sensor Clock pin. External pull up resistor is required when using in cascade application or connecting to I^2C slave. The corresponding pins must be connected to the master chip for cascade application.	GND

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	MOSFET Driver	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and GND in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and GND in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and GND in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and GND in the application circuit.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL. Connect a stabilizing capacitor between VSL and GND in the application circuit.	-
VCOM	C	Panel & Stabilizing capacitor	VCOM driving signal	This pin is VCOM driving volage, VCOM. Connect a stabilizing capacitor between VCOM and GND in the application circuit.	-

Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [399:0]	O	Panel	Source driving signal	Source output pin.	Open
G [299:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open

Table 5-5: Other Pins

Name	Type	Connect to	Function	Description	When not in use
TIN	I	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
TPE	O	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
CL	I/O	Open	Reserved	Reserved	Open
RSV	NC	NC	Reserved	This is a reserved pin and should be kept open.	Open
TPA, TPB, TPC, TPD, TPF	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPE, TPF and TIN.	Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD2683 can support 3-wire/4-wire serial peripheral. In the SSD2683, the MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1: Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	DC	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

Note

(1) L is connected to GND and H is connected to V_{DDIO}

6.1.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC and CSB. The control pins status in 4-wire SPI in reading/writing command/data is shown in

Table 6-2.

The read/write procedure of 4-wire SPI is shown in Figure 6-1.

Table 6-2: Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of DC should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to DC pin.

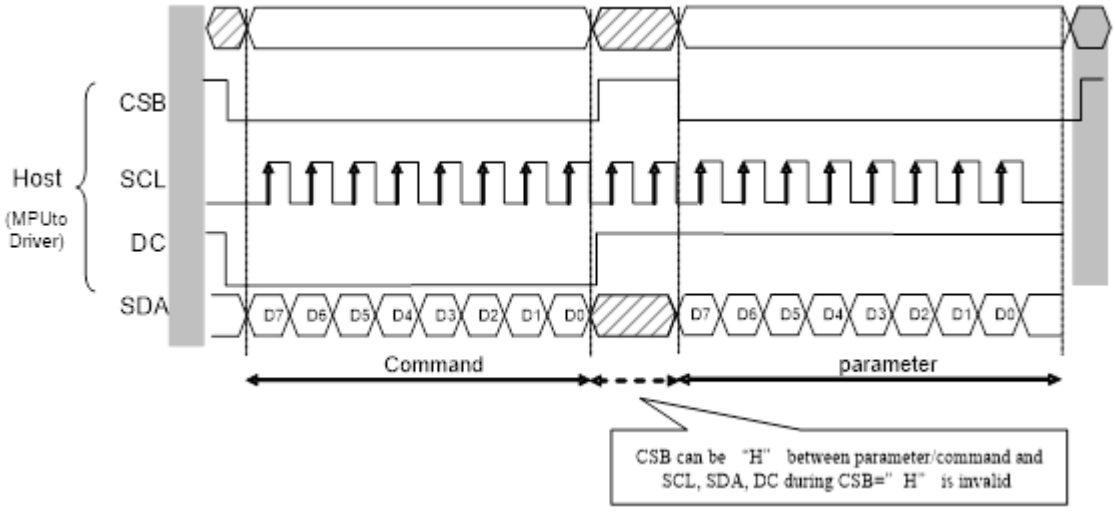


Figure 6-1: Read/Write procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while DC pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the read/write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is DC bit, D7 bit, D6 bit to D0 bit. The first bit is DC bit which determines the following byte is command or data. When DC bit is 0, the following byte is command. When DC bit is 1, the following byte is data. The read/write procedure of 3-wire SPI is shown in Figure 6-2.

Table 6-3: Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

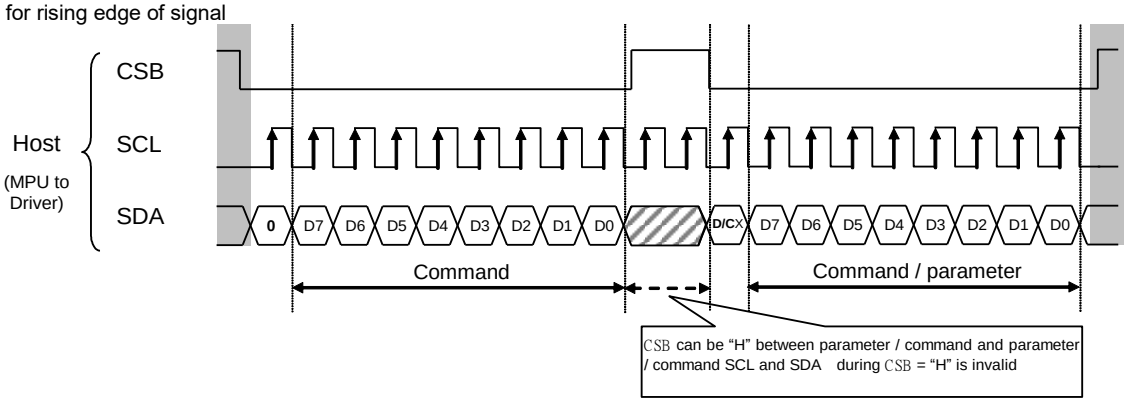


Figure 6-2: Read/Write procedure in 3-wire SPI mode

6.2 RAM

The On-chip display RAM is holding the image data. 2bpp for 400x300 resolution.

6.3 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

6.4 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

6.5 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into MTP. It required PON with DCVCOM mode for analog voltage ready.

The typical flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Sources are GND.
- VCOM pin is used for sensing.
- During Sensing period, BUSY_N is kept flagged.
- After Sensing, Active Gate return to non-select stage.

6.6 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.

TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1) If the Temperature value MSByte bit D11 = 0, then
   the temperature is positive and value (DegC) = + (Temperature value) / 16
2) If the Temperature value MSByte bit D11 = 1, then
   the temperature is negative and value (DegC) = - (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
1100 1001 0000	C90	-880	-55
1100 1001 0010	C92	-878	-54.875
1110 0111 0000	E70	-400	-25
1111 1111 1110	FFE	-2	-0.125
0000 0000 0000	0	0	0
0000 0000 0010	2	2	0.125
0001 1001 0000	190	400	25
0111 1101 0000	7D0	2000	125
0111 1110 0010	7E2	2018	126.125
0111 1110 1110	7EE	2030	126.875
0111 1111 0000	7F0	2032	127

6.7 Cascade Mode

The SSD2683 has a cascade mode that can cascade 2 chips to achieve the higher display resolution. The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to GND, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its booster and regulator circuit will be disabled. The analog voltages will come from the master chip. Therefore, the corresponding pins including TSDA, TSCL, SYNC[0:1], VCORE, VGH, VGL, VSH1, VSL, VSH2 and VCOM must be connected to the master chip.

7 COMMAND TABLE

7.1 User Command Table

Table 7-1: Summary of user command table

R/W	D/CX	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR
W	0	00h	PSR Panel Setting Register	0	0	0	0	0	0	0	0	
W	1			RES[1:0]		B_mode	0	UD	SHL	SHD_N	RST_N	2Fh
W	1			LUT_EN	FOPT[1:0]		VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
W	0	01h	PWR Power setting Register	0	0	0	0	0	0	0	1	
W	1			0	0	0	0	0	VSC_EN	VS_EN	VG_EN	07h
W	1			1	1	1	1	0	0	VGPN[1:0]		F0h
W	1			0	VSPL[6:0]							00h
W	1			0	VSNL[6:0]							00h
W	1			0	VSPL2[6:0]							00h
W	1			0	VSNL2[6:0]							00h
W	0	02h	POF Power OFF Command	0	0	0	0	0	0	1	0	
W	1			00h								-
W	0	03h	POFS Power off Sequence Setting	0	0	0	0	0	0	1	1	
W	1			0	0	T_VDPG_OFF[1:0]		0	0	T_VDS_OFF[1:0]		00h
W	0	04h	PON Power ON Command Register	0	0	0	0	0	1	0	0	
W	0	06h	BTST Booster Soft Start Setting Register	0	0	0	0	0	1	1	0	
W	1			0	VGHSSC_ONT[2:0]			T_VGHSSA[1:0]		T_VGHSSB[1:0]		0Fh
W	1			1	VGHSSA_DRV[2:0]			VGHSSA_OFFT[[3:0]				8Bh
W	1			1	VGHSSB_DRV[2:0]			VGHSSB_OFFT[[3:0]				9Ch
W	1			1	VGHSSC_DRV[2:0]			VGHSSC_OFFT[[3:0]				96h
W	0	07h	DSLP Deep Sleep Register	0	0	0	0	0	1	1	1	
W	1			A5h								-
W	0	10h	DTM Data Start transmission Register	0	0	0	1	0	0	0	0	
W	1			KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		-
W	1			..	..	..	..	..	..	..	..	-
W	1			Kpixel(4M-3)[1:0]		Kpixel(4M-2)[1:0]		Kpixel(4M-1)[1:0]		Kpixel(4M)[1:0]		-
W	0	12h	DRF Display Refresh Command Register	0	0	0	1	0	0	1	0	
W	1			00h								-
W	0	17h	AUTO Auto Sequence Register	0	0	0	1	0	1	1	1	
W	1			A5h or A7h								-
W	0	30h	PLL Frame Rate Control register	0	0	1	1	0	0	0	0	
W	1			0	0	0	0	0	FR[2:0]			02h
W	0	40h	TSC. Temperature Sensor Command Register	0	1	0	0	0	0	0	0	
R	1			TS[7:0]								-
W	0	41h	TSE Temperature Sensor Enable Register	0	1	0	0	0	0	0	1	
W	1			TSE	0	0	0	TO[3:1]			0	00h
W	0	42h	TSW Temperature Sensor Write Register	0	1	0	0	0	0	1	0	
W	1			WATTR[7:0]								00h
W	1			WMSB[7:0]								00h
W	1			WLSB[7:0]								00h
W	0	43h	TSR Temperature Sensor Read Register	0	1	0	0	0	0	1	1	
R	1			RMSB[7:0]								-
W	0	50h	CDI VCOM and DATA interval setting Register	0	1	0	1	0	0	0	0	
W	1			VBD[2:0]			DDX	CDI[3:0]				97h
W	0	51h	LPD Lower Power Detection Register	0	1	0	1	0	0	0	1	
R	1			0	0	0	0	0	0	0	LPDstatus	
W	0	61h	TRES Resolution setting Register	0	1	1	0	0	0	0	1	
W	1			0	0	0	0	0	0	0	HRES[8]	01h
W	1			HRES[7:0]								90h
W	1			0	0	0	0	0	0	0	VRES[8]	01h
W	1			VRES[7:0]								2Ch
W	0	65h	GSST Gate/Source Start Setting Register	0	1	1	0	0	1	0	1	
W	1			0	0	0	0	0	0	0	S_start[8]	00h
W	1			S_start[7:0]								00h
W	1			0	0	0	0	0	0	0	G_start[8]	00h
W	1			G_start[7:0]								00h

R/W	D/CX	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR
W	0	70h	REV Chip Revision Register	0	1	1	1	0	0	0	0	
R	1			A[7:0]								06h
R	1			B[7:0]								01h
R	1			C[7:0]								01h
W	0	80h	AMV Auto Measurement VCOM Register	1	0	0	0	0	0	0	0	
W	1			P[1:0]		AMVT[1:0]		AMVX	AMVS	0	AMVE	00h
W	0	81h	VV VCOM Value Register	1	0	0	0	0	0	0	1	
R	1			1	0	VV[5:0]						-
W	0	82h	VDCS VCM_DC Setting Register	1	0	0	0	0	0	1	0	
W	1			MTP_VCM	VDCS[6:0]							00h
W	0	83h	PTLW PARTIAL WINDOW	1	0	0	0	0	0	1	1	
W	1			0	0	0	0	0	0	0	HRST[8]	00h
W	1			HRST[7:0]								00h
W	1			0	0	0	0	0	0	0	HRED[8]	01h
W	1			HRED[7:0]								8Fh
W	1			0	0	0	0	0	0	0	VRST[8]	00h
W	1			VRST[7:0]								00h
W	1			0	0	0	0	0	0	0	VRED[8]	01h
W	1			VRED[7:0]								2Bh
W	1			0	0	0	0	0	0	#	PMODE	00h
W	0	90h	PGM Program Mode	1	0	0	1	0	0	0	0	
W	0	91h	APG Active Program	1	0	0	1	0	0	0	1	
W	0	92h	RMTP Read MTP Data	1	0	0	1	0	0	1	0	
R	1			dummy byte								-
R	1			Address 0 in MTP								-
R	1			...								-
R	1			Address n in MTP								-
W	0	E0h	CCSET Temperature input selection	1	1	1	0	0	0	0	0	
W	1			0	0	0	0	0	0	TSFIX	0	00h
W	0	E3h	PWS Power Saving Register	1	1	1	0	0	0	1	1	
W	1			VCOM_W[3:0				SD_W[3:0]				65h
W	0	E4h	LVSEL LVD Voltage Select Register	1	1	1	0	0	1	0	0	
W	1			0	0	0	0	0	0	LVD_SEL[1:0]		03h
W	0	E6h	TSSET Manual input temperature value	1	1	1	0	0	1	0	0	
W	1			TS_SET[7:0]								00h

Note:

(1) The bit which has been written as “0” or ”1” in Table 7-1 must be followed. Otherwise, device malfunction may occur.
(2) The driver IC will not response to all read & write commands during BUSY_N=0.
(3) Commands are only effective while all corresponding parameters for that command were written completely.
(4) Commands or parameters not shown on above table are for “Reserve” usage.
(5) POR value may be changed without notice.

8 Command Table Description

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 2Fh [POR] B[7:0] = 09h [POR]
0	1		A_7	A_6	A_5	0	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: Follow TRES setting: 400x300 (Default) 01b: 320x300 10b: 300x240 11b: 200x300 *Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power. A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 … G0 1: Scan up. (Default) First line to Last line: G0 … Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 … S0 1: Shift right. (Default) First data to Last data: S0 … Sn-1 A[1] ~ SHD_N Booster Switch: 0 : Booster off, register data are kept, and Source/VBD/ Vcom are kept 0V or floating. 1 : Booster on. (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N will output low during operation.

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7] ~ LUT_EN 0: During reset, auto load LUT from MTP if it is valid. When PON/DRF, analog setting will follow the content of MTP. (Default) 1: During reset, no action to load LUT from MTP. When PON/DRF, analog setting will follow the content of MCU B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating) B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating. B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading MTP, Temperature Sensor will be activated automatically one time. (default) B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND. B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>PWR</td><td>Power setting Register
A[5:0] = 07h [POR]
B[7:0] = F0h [POR]
C[6:0] = 00h [POR]
D[6:0] = 00h [POR]
E[6:0] = 00h [POR]
F[6:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[2] ~ VSC_EN
Source LV power selection:
0: External source power for VSH2 pin.
1: Internal DCDC function for generate source power. (default)
A[1] ~ VS_EN
Source LV power selection:
0: External source power for VSH1 and VSL pin.
1: Internal DCDC function for generate source power. (default)
A[0] ~ VG_EN
Gate power selection:
0: External gate power for VGH and VGL pin.
1: Internal DCDC function for generate gate power. (default)</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>B_1</td><td>B_0</td><td></td><td>B[1:0] ~ VGPN [1:0]
Internal VGH / VGL Voltage Level Selection:
<table>
<tr><th>VGPN [1:0]</th><th>Gate Voltage Level</th></tr>
<tr><td>00</td><td>VGH=20V,VGL=-20V (Default)
VSH=15V, VSL=-15V</td></tr>
<tr><td>01</td><td>VGH=17V ,VGL=-17V
VSH=15V, VSL=-15V</td></tr>
<tr><td>10</td><td>VGH=15V,VGL=-15V
VSH=13V, VSL=-13V</td></tr>
<tr><td>11</td><td>Reserved.</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td><td></td><td>C[6:0] ~ VSPL [6:0]
Internal Source Voltage Level Selection for VSH2@Mode0:
<table>
<tr><th>VSPL[6:0]</th><th>Voltage Level</th></tr>
<tr><td>00h</td><td>3.0V (default)</td></tr>
<tr><td>02h</td><td>3.2V</td></tr>
<tr><td>04h</td><td>3.4V</td></tr>
<tr><td>06h</td><td>3.6V</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>76h</td><td>14.8V</td></tr>
<tr><td>78h</td><td>15.0V</td></tr>
<tr><td>Other</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td></td><td>D[6:0] ~ VSNL[6:0]
Internal Source Voltage Level Selection for VSL@Mode1:
<table>
<tr><th>VSNL[6:0]</th><th>Voltage Level</th></tr>
<tr><td>00h</td><td>-3.0V (default)</td></tr>
<tr><td>02h</td><td>-3.2V</td></tr>
<tr><td>04h</td><td>-3.4V</td></tr>
<tr><td>06h</td><td>-3.6V</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>76h</td><td>-14.8V</td></tr>
<tr><td>78h</td><td>-15.0V</td></tr>
<tr><td>Other</td><td>Reserved</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>E_6</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td><td></td><td>E[6:0] ~ VSPL2[6:0]
Internal Source Voltage Level Selection for VSH1@Mode1:
<table><tr><th>VSPL2[6:0]</th><th>Voltage Level</th></tr><tr><td>00h</td><td>3.0V (default)</td></tr><tr><td>02h</td><td>3.2V</td></tr><tr><td>04h</td><td>3.4V</td></tr><tr><td>06h</td><td>3.6V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>76h</td><td>14.8V</td></tr><tr><td>78h</td><td>15.0V</td></tr><tr><td>Other</td><td>Reserved</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td><td></td><td>F[6:0] ~ VSNL2[6:0]
Internal Source Voltage Level Selection for VSH2@Mode1:
<table><tr><th>VSNL2[6:0]</th><th>Voltage Level</th></tr><tr><td>00h</td><td>3.0V (default)</td></tr><tr><td>02h</td><td>3.2V</td></tr><tr><td>04h</td><td>3.4V</td></tr><tr><td>06h</td><td>3.6V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>76h</td><td>14.8V</td></tr><tr><td>78h</td><td>15.0V</td></tr><tr><td>Other</td><td>Reserved</td></tr></table></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>02</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>POF</td><td>Power OFF Command Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>After power off command, driver will power off based on the Power OFF Sequence. BUSY_N will output low during operation.

The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off.
SD output will base on previous condition.
*Remark: POF works at PON only</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>POFS</td><td>Power on/off Sequence Setting Register
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>A[5:4] ~ T_VDPG_OFF[1:0]
Power off delay from VGH to VGL
00b: 20ms (default)
01b: 40ms
10b: 60ms
11b: 80ms

A[1:0] ~ T_VDS_OFF[1:0]
Power off delay from VSHX/VSL to VGH
00b: 20ms (default)
01b: 40ms
10b: 60ms
11b : 80ms</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>PON</td><td>Power ON Command Register
After the Power ON command, driver will power on based on the Power ON Sequence.
BUSY_N will output low during operation.

* Remark:
PON Include booster on, VSH1/VSH2/VSL regulator on
With default BTST, timing is >80ms</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>06</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>BTST</td><td>VGH Booster Soft Start Setting Register (for VGH)
A[6:0] = 0Fh [POR]
B[6:0] = 8Bh [POR]
C[6:0] = 9Ch [POR]
D[6:0] = 96h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td rowspan="4">A[6:4] ~ VGHSSC_ONT [2:0]
VGH booster maximum MOSFET ON time (reserved)
A[6:4] = 000 (Default)

A[3:2] ~ T_VGHSSA [1:0] = 11 (Default)
VGH booster soft start Phase A duration
A[1:0] ~ T_VGHSSB [1:0] = 11 (Default)
VGH booster soft start Phase B duration
<table><tr><th></th><th>Soft Start Phase Period (ms)</th></tr><tr><td>00</td><td>10</td></tr><tr><td>01</td><td>20</td></tr><tr><td>10</td><td>30</td></tr><tr><td>11</td><td>40</td></tr></table>
B[6:4] ~ VGHSSA_DRV [2:0] = 000 (Default)
VGH Phase A Driving Strength
C[6:4] ~ VGHSSB_DRV [2:0] = 001 (Default)
VGH Phase B Driving Strength
D[6:4] ~ VGHSSC_DRV [2:0] = 001 (Default)
VGH Phase C Driving Strength
<table><tr><th colspan="4">Driving Strength</th></tr><tr><td>000</td><td>0</td><td>100</td><td>(reserved)</td></tr><tr><td>001</td><td>1</td><td>101</td><td>(reserved)</td></tr><tr><td>010</td><td>2</td><td>110</td><td>(reserved)</td></tr><tr><td>011</td><td>3(strongest)</td><td>111</td><td>(reserved)</td></tr></table>
B[3:0] ~ VGHSSA_OFFT[[3:0] = 1011 (Default)
VGH Phase A Minimum OFF Time
C[3:0] ~ VGHSSB_OFFT[[3:0] = 1100 (Default)
VGH Phase B Minimum OFF Time
D[3:0] ~ VGHSSC_OFFT[[3:0] = 0110 (Default)
VGH Phase C Minimum OFF Time
<table><tr><th colspan="4">Minimum OFF Time (setting)</th></tr><tr><td>0000</td><td>OFFH0</td><td>1000</td><td>OFFH8</td></tr><tr><td>0001</td><td>OFFH1</td><td>1001</td><td>OFFH9</td></tr><tr><td>0010</td><td>OFFH2</td><td>1010</td><td>OFFHA</td></tr><tr><td>0011</td><td>OFFH3</td><td>1011</td><td>OFFHB</td></tr><tr><td>0100</td><td>OFFH4</td><td>1100</td><td>OFFHC</td></tr><tr><td>0101</td><td>OFFH5</td><td>1101</td><td>OFFHD</td></tr><tr><td>0110</td><td>OFFH6</td><td>1110</td><td>OFFHE</td></tr><tr><td>0111</td><td>OFFH7</td><td>1111</td><td>OFFHF</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>07</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>DSLP</td><td>Deep Sleep Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td></td><td>This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion.
The only one parameter is a check code, the command would be executed if check code is A5h.</td></tr>
<tr><td colspan="13"></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DTM</td><td>Data Start transmission Register</td></tr>
<tr><td colspan="10">2 bit per pixel</td><td rowspan="5">This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

KPixel[1:0] Source Driver Output
<table><tr><th></th><th>DDX=1 (Default)</th><th>DDX=0</th></tr><tr><td>00b</td><td>Gray 0</td><td>Gray 3</td></tr><tr><td>01b</td><td>Gray 1</td><td>Gray 2</td></tr><tr><td>10b</td><td>Gray 2</td><td>Gray 1</td></tr><tr><td>11b</td><td>Gray 3</td><td>Gray 0</td></tr></table>
After issue this command, the host must send at least 1-byte data to the device.</td></tr>
<tr><td>0</td><td>1</td><td></td><td colspan="4">KPixel1 [1:0]</td><td colspan="3">KPixel2 [1:0]</td><td colspan="2">KPixel3 [1:0]</td><td>KPixel4 [1:0]</td></tr>
<tr><td>:</td><td></td><td></td><td colspan="10">…</td></tr>
<tr><td>0</td><td>1</td><td></td><td colspan="4">KPixel (4M-3) [1:0]</td><td colspan="3">KPixel (4M-2) [1:0]</td><td colspan="2">KPixel (4M-1) [1:0]</td><td>KPixel (4M) [1:0]</td></tr>
<tr><td colspan="10"></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>DRF</td><td>Display Refresh Command Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.
BUSY_N will output low during operation.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>AUTO</td><td>Auto Sequence Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>This command makes the chip enter the auto sequence
Single-chip application ONLY.
Auto Sequence Option
0xA5: Start Auto Sequence (PON > DRF > POF)
0xA7: Start Auto Sequence (PON > DRF > POF > DSLP).
Others: No effect
BUSY_N will output low during operation.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>30</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PLL</td><td>Frame Rate Control register
The command controls the clock frequency.
A[3:0] = 2h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[3] ~ Dyna
Dynamic Frame Rate
0: Disable (Default)
1: Enable

A[2:0] ~ FR[2:0]
It supports the following frame rates.
Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.
<table><tr><th>FR[2:0]</th><th>Frame Rate Selection</th></tr><tr><td>000</td><td>12.5Hz</td></tr><tr><td>001</td><td>25Hz</td></tr><tr><td>010</td><td>50Hz (Default)</td></tr><tr><td>011</td><td>65Hz</td></tr><tr><td>100</td><td>75Hz</td></tr><tr><td>101</td><td>85Hz</td></tr><tr><td>110</td><td>100Hz</td></tr><tr><td>111</td><td>120Hz</td></tr></table></td></tr>
<tr><td colspan="13"></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>40</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>TSC</td><td>Temperature Sensor Command Register</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>This command enables internal temperature sensor.
BUSY_N will output low during operation.
Then the temperature value can be read in 1degC step
A[7:0] ~ TS [7:0]
<table>
<tr><th>TS [7:0]</th><th>Return Value(degC)</th></tr>
<tr><td>E7h</td><td>-25</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>FFh</td><td>-1</td></tr>
<tr><td>00h</td><td>0</td></tr>
<tr><td>01h</td><td>1</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>19h</td><td>25</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>31h</td><td>49</td></tr>
<tr><td>32h</td><td>50</td></tr>
</table></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>41</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>TSE</td><td>Temperature Sensor Enable Register
This command selects Temperature offset
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>0</td><td></td><td>A[3:0] ~ TO[3:1] , Temperature offset:
<table>
<tr><th>TO[3:1]</th><th>Calculation</th><th>TO[3:1]</th><th>Calculation</th></tr>
<tr><td>000</td><td>+0</td><td>100</td><td>-4</td></tr>
<tr><td>001</td><td>+1</td><td>101</td><td>-3</td></tr>
<tr><td>010</td><td>+2</td><td>110</td><td>-2</td></tr>
<tr><td>011</td><td>+3</td><td>111</td><td>-1</td></tr>
</table></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>50</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CDI</td><td>VCOM and DATA interval setting Register
This command indicates the Border Output Selection and the interval between Vcom and data output
A[7:0] = 97h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[7:5]~VBD [2:0]
Border Output Selection:
<table>
<tr><th></th><th>DDX=1</th><th>DDX=0</th></tr>
<tr><td>VBD[2:0]</td><td>LUT (Default)</td><td>LUT</td></tr>
<tr><td>000</td><td>Gray 0</td><td>HIZ</td></tr>
<tr><td>001</td><td>Gray 1</td><td>Gray 3</td></tr>
<tr><td>010</td><td>Gray 2</td><td>Gray 2</td></tr>
<tr><td>011</td><td>Gray 3</td><td>Gray 1</td></tr>
<tr><td>100</td><td>HIZ(Default)</td><td>Gray 0</td></tr>
</table>
A[4]: DDX
Data Polarity for Pixel Data (See DTM command)
0: Invert
1: Non-invert (Default)
A[3:0] ~ CDI[3:0]
Gate and source blanking time (No gate source scanning)
<table>
<tr><th>CDI [3:0]</th><th>Interval (ms)</th><th>CDI [3:0]</th><th>Interval (ms)</th></tr>
<tr><td>0h</td><td>2</td><td>8h</td><td>40</td></tr>
<tr><td>1h</td><td>4</td><td>9h</td><td>60</td></tr>
<tr><td>2h</td><td>8</td><td>Ah</td><td>80</td></tr>
<tr><td>3h</td><td>12</td><td>Bh</td><td>100</td></tr>
<tr><td>4h</td><td>14</td><td>Ch</td><td>120</td></tr>
<tr><td>5h</td><td>16</td><td>Dh</td><td>140</td></tr>
<tr><td>6h</td><td>18</td><td>Eh</td><td>160</td></tr>
<tr><td>7h</td><td>20 (Default)</td><td>Fh</td><td>Reserved</td></tr>
</table>
User needs to review CDI setting to have stable VCOM in application</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>51</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>LPD</td><td>Lower Power Detection Register</td></tr>
<tr><td>1</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_0</td><td></td><td>BUSY_N will output low during operation.
Then the LPD status can be read.
A[0] ~ LPD status
0: Low power input
VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL
1: Normal (default)</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>61</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>TRES</td><td>Resolution setting Register
A[9:0] = 190h [POR]
B[9:0] = 12Ch [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td><td></td><td rowspan="5">This command defines alternative resolution
A[9]=0b,
A[8:0] ~ HRES[8:0]
Horizontal Display Resolution
Remark: Horizontal resolution should be 4-multiple.
B[9]=0b,
B[8:0] ~ VRES[8:0]
Vertical Display Resolution

e.g. HRES= 190h, VRES= 12Ch
<table><tr><th>UD,SHL</th><th>Source and gate sequence</th></tr><tr><td>00</td><td>S399,G299 to S0,G0</td></tr><tr><td>01</td><td>S0, G299 to S399,G0</td></tr><tr><td>10</td><td>S399,G0 to S0, G299</td></tr><tr><td>11</td><td>S0,G0 to S399, G299</td></tr></table>Remark:
1) Both PSR.RES & TRES command can set panel resolution. Priority will be given to the last received PSR or TRES command.
2) TRES is selected when PSR.RES=2’b00
3) VRES[8:0] >= 152</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_9</td><td>B_8</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>65</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>GSST</td><td>Gate/Source Start Setting Register.
A[9:0] = 000h [POR]
B[9:0] = 000h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td><td></td><td rowspan="5">A[9]=0b, A[8:0] ~ S_start[8:0]
First valid source output channel setting
<table><tr><th>S_start [7:0]</th><th>First valid source output</th></tr><tr><td>00h</td><td>S0 (Default)</td></tr><tr><td>04h</td><td>S4</td></tr><tr><td>08h</td><td>S8</td></tr><tr><td>…</td><td>…</td></tr><tr><td>188h</td><td>S392</td></tr><tr><td>18Ch</td><td>S396</td></tr><tr><td>Other</td><td>Reserved</td></tr></table>B[9]=0b, B[8:0] ~ G_start[8:0]
First valid gate output channel setting

GSST and TRES can define the display window from target source and gate start and end line.
Eg. GD: First G active = G16, G_start[8:0]=16.
Last G active = G279, VRES[8:0]=264.
SD: First S active = S8, S_start[7:0]=8.
Last S active = S167, HRES[7:0]=160.
Remark:
1) PSR.RES[1:0] = 00
2) G_start+VRES< 300, S_start+HRES< 400.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_9</td><td>B_8</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td><td></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>70</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="4">REV</td><td rowspan="4">Chip Revision Register
The command is to read the ID
A[7:0] = 06h [POR]
B[7:0] = 01h [POR]
C[7:0] = 01h [POR]</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>1</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>80</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">AMV</td><td>Auto Measurement VCOM Register
This command implements related VCOM sensing setting.
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>0</td><td>A_0</td><td>A[7:6] ~ P[1:0]
Number of sensing Points
00: 2 (Default)
01: 4
10: 8
11: 16

A[5:4] ~AMVT[1:0]
Auto Measure Vcom Time:
Sensing Time
00: 5 sec. (Default)
01: 10 sec.
10: 15 sec.
11: 20 sec.

A[3] ~ AMVX
VCOM measurement Gate settings
0: Gate scan normally during VCOM measurement (Default)
1: All Gates ON during VCOM measurement
A[2] ~ AMVS
Source output of AMV:
0: Set Source output to 0V during Auto Measure VCOM period. (Default)
1: Set Source output to VSH_LV during Auto Measure VCOM period.

A[0] ~ AMVE
Auto Measure Vcom Enable (/Disable):
0: Disabled (Default)
1: Enabled
BUSY_N will output low during operation.

Note: AMV works at PON only</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>81</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">VV</td><td>Auto Measurement VCOM Register
This command gets the Vcom value after AMV.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>1</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>A[5:0] ~ VV[5:0]:
Vcom read Value, valid range from -0.2V to -3.0V.
<table>
<tr><th>VV[5:0]</th><th>Vcom read value</th></tr>
<tr><td>00h</td><td>Reserved</td></tr>
<tr><td>04h</td><td>-0.2V</td></tr>
<tr><td>08h</td><td>-0.4V</td></tr>
<tr><td>0Ch</td><td>-0.6V</td></tr>
<tr><td>10h</td><td>-0.8V</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>3Ch</td><td>-3.0V</td></tr>
<tr><td>others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td colspan="13"></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>82</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>VDCS</td><td>VCM_DC Setting Register
This command sets VCOM_DC value.
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>0</td><td>0</td><td></td><td>A[7] ~ MTP_VCM
Vcom follow VDCS after RESET.
0: Disable (Default), auto load from MTP if it is valid.
1: Enable, VCOM value from the VDCS[6:0]

A[6:0] ~ VDCS[6:0]:
VCOM_DC Setting, 0.2V step from -0.2V to -3V.
<table>
<tr><th>VDCS [6:0]</th><th>VCOM_DC Setting</th></tr>
<tr><td>00h</td><td>Reserved</td></tr>
<tr><td>04h</td><td>-0.2V</td></tr>
<tr><td>08h</td><td>-0.4V</td></tr>
<tr><td>0Ch</td><td>-0.6V</td></tr>
<tr><td>10h</td><td>-0.8V</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>3Ch</td><td>-3.0V</td></tr>
<tr><td>others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>83</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>PTLW</td><td>PARTIAL WINDOW
This command sets partial window address.
A[9:0] = 000h [POR]
B[9:0] = 18Fh [POR]
C[9:0] = 000h [POR]
D[9:0] = 12Bh [POR]
E[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td><td></td><td rowspan="10">A[9]=0b,
A[8:0] ~ HRST [8:0]
Horizontal start address
B[9]=0b,
B[8:0] ~ HRED [8:0]
Horizontal end address
C[9]=0b,
C[8:0] ~ VRST [8:0]
Vertical start address
D[9]=0b,
D[8:0] ~ VRED [8:0]
Vertical end address

E[0] ~ PMODE
0: disable partial mode (Default)
1: enable partial mode
Gate scan both inside and outside of the partial window

Requirement:
1) HRST [8:0]<= HRED [8:0]
2) VRST [8:0]<= VRED [8:0]
3) HRST/HRED step size = 4,
HRST [1:0] = 2b’00, HRED [1:0] = 2’b11</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_9</td><td>B_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C_9</td><td>C_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D_9</td><td>D_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>E_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>90</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PGM</td><td>Program Mode
This command is to set MTP program mode
After this command is issued, the chip would enter the program mode.
After the programming procedure completed, a hardware reset is necessary for leave the program mode
BUSY_N will output low until PGM mode is ready.</td></tr>
</table>

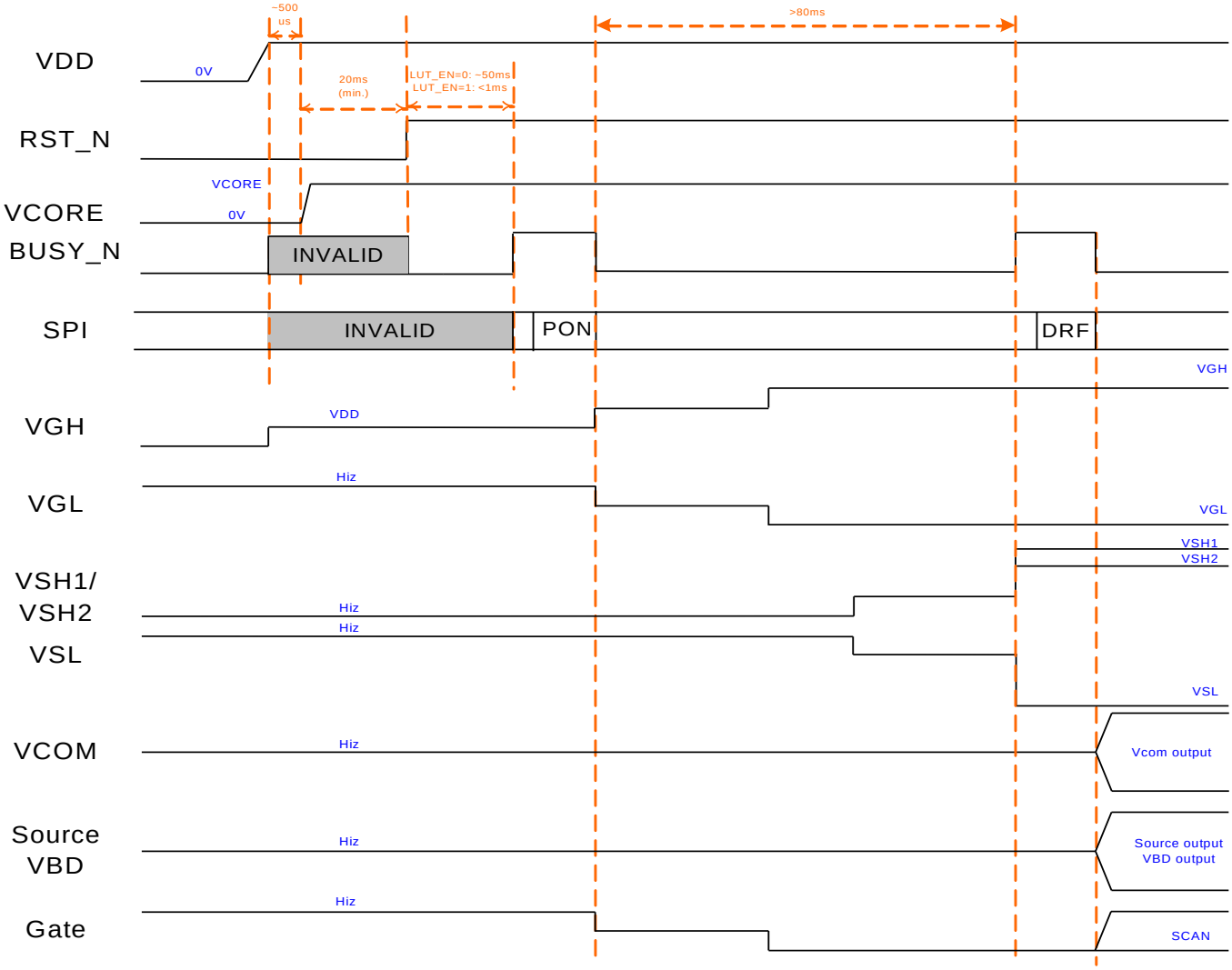
<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>91</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>APG</td><td>Active Program
This command is to execute MTP program
After this command is issued, the chip would program the MTP.
BUSY_N will output low during operation.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>92</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">RMTP</td><td>Read MTP Data</td></tr>
<tr><td>1</td><td>1</td><td></td><td colspan="9">1st ~ dummy
2nd ~ N+1th Parameter</td><td>This command is to read the MTP content from SRAM.
The 1st byte read is dummy byte.
The 2nd byte read is the content of Address 0 in MTP
The N+1th byte read is the content of Address n in MTP
After issue this command, the host must read at least 1 byte data from the device.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">CCSET</td><td>CCSET for temperature input selection
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>0</td><td>A[1] = TSFIX
Temperature Input selection
0: Use Internal Temperature sensor (Default)
1: Use TSSET[7:0] value
A[0] = CSEIN, cascade mode enable
0: Disable
1: Enable</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E3</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">PWS</td><td>Power Saving Register
This command is sets for saving power VCOM/Source power saving during display refresh period.
A[7:0] = 65h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

A[7:4] = VCOM_W [3:0]
<table>
<tr><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th></tr>
<tr><td>0</td><td>Reserved</td><td>8</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>9</td><td>9</td></tr>
<tr><td>2</td><td>2</td><td>10</td><td>10</td></tr>
<tr><td>3</td><td>3</td><td>11</td><td>11</td></tr>
<tr><td>4</td><td>4</td><td>12</td><td>12</td></tr>
<tr><td>5</td><td>5</td><td>13</td><td>13</td></tr>
<tr><td>6</td><td>6[Default]</td><td>14</td><td>14</td></tr>
<tr><td>7</td><td>7</td><td>15</td><td>15</td></tr>
</table>
A[3:0] = SD_W [3:0]
<table>
<tr><th>SD_W [3:0]</th><th>Source power saving width[us]</th><th>SD_W [3:0]</th><th>Source power saving width [us]</th></tr>
<tr><td>0</td><td>Reserved</td><td>8</td><td>4</td></tr>
<tr><td>1</td><td>0.5</td><td>9</td><td>4.5</td></tr>
<tr><td>2</td><td>1</td><td>10</td><td>5</td></tr>
<tr><td>3</td><td>1.5</td><td>11</td><td>5.5</td></tr>
<tr><td>4</td><td>2</td><td>12</td><td>6</td></tr>
<tr><td>5</td><td>2.5[Default]</td><td>13</td><td>6.5</td></tr>
<tr><td>6</td><td>3</td><td>14</td><td>7</td></tr>
<tr><td>7</td><td>3.5</td><td>15</td><td>7.5</td></tr>
</table></td></tr>
</table>

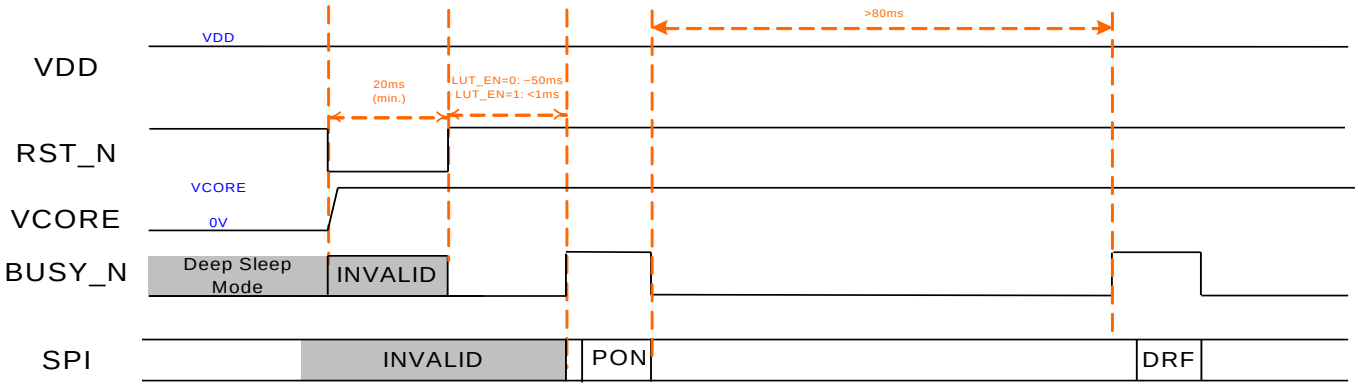
<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Remark:
VCOM_W setting < CDI setting
SD_W setting < S2G setting</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E4</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>LVSEL</td><td>LVD Voltage Select Register
This command is sets for low power detect level power
A[1:0] = 3h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>A[1:0] ~ LVD_SEL[1:0]
Low power detection threshold
00: 2.2V
01: 2.3V
10: 2.4V
11 : 2.5V (Default)</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>E6</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>TSSET</td><td>Manual input temperature value
This command is to force the TS value
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[7:0] ~ TS_SET[7:0]
When TSFIX=1, Temperature value will be set by TS_SET[7:0].
Format of the temperature value is 8-bit binary value and it is 1degC per step.
<table>
<tr><th>TS_SET[7:0]</th><th>Force the TS Value(degC)</th></tr>
<tr><td>E7h</td><td>-25</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>FFh</td><td>-1</td></tr>
<tr><td>00h</td><td>0</td></tr>
<tr><td>01h</td><td>1</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>19h</td><td>25</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>31h</td><td>49</td></tr>
<tr><td>32h</td><td>50</td></tr>
</table></td></tr>
</table>

9 Display on/off Sequence

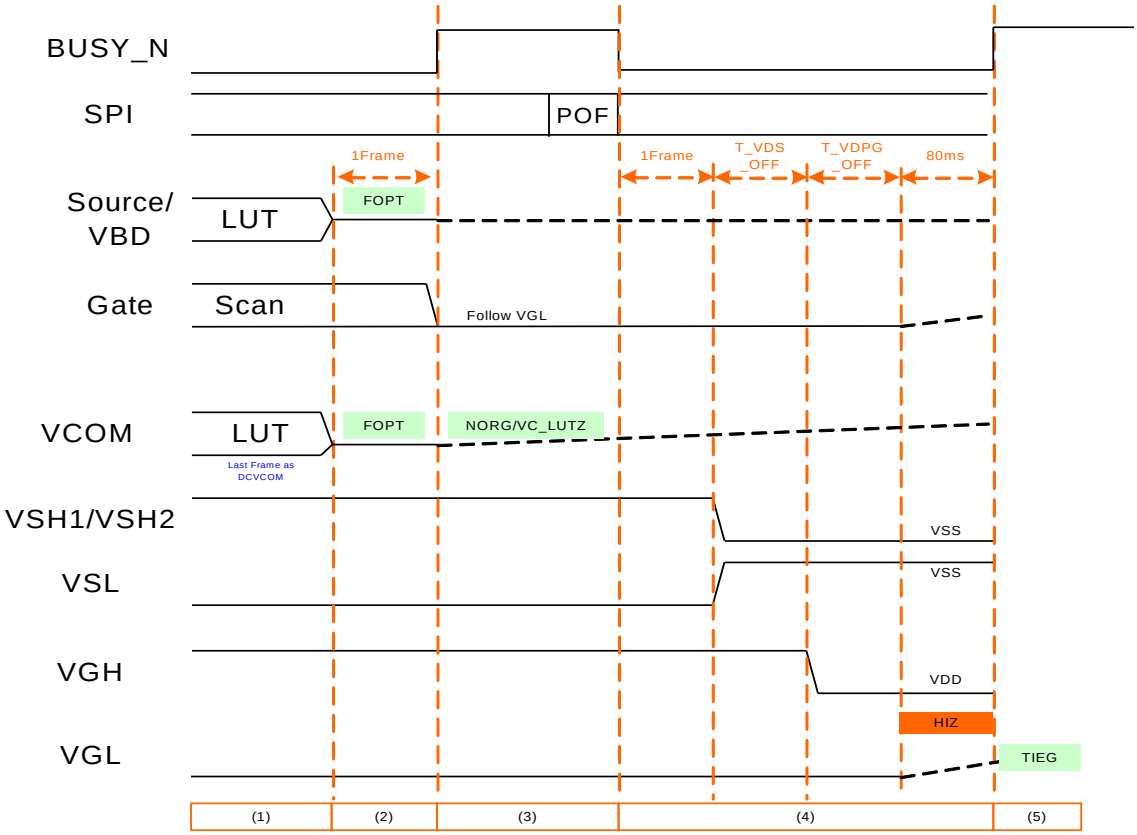
9.1 Display on sequence from VDD power on



9.2 Display on sequence from deep sleep mode



9.3 Display off Sequence Display



Note: If VCOM and VGL set as floating after display update. Please wait until the system completely discharge before next operation.

10 Absolute Maximum Rating

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-30 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VDD be constrained to the range GND < VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, T_{OPR}=25ºC.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	VDD supply operation voltage	VDD		2.3	3.0	3.6	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-3.0	-	-0.2	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM	No output load	-200	-	200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL}	V_{COM_DC}	V_{SH}	V
V_{GATE}	Gate output voltage	G0~G295		-20	-	+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G295		-	-	40	V
VSH	Positive Source output voltage	VSH1		+3		+15	V
VSH2	Positive Source output voltage	VSH2		+3		+15	V
dV_{SH}	VSH1/VSH2 output voltage deviation	VSH1/ VSH2	No output load	-200	-	200	mV
V_{SL}	Negative Source output voltage	VSL		-15		-3	V
dV_{SL}	VSL output voltage deviation	VSL	No output load	-200	-	200	mV
V_{IH}	High level input voltage	SDA SCL, CSB, DC, RST_N, BS1, M/S#		0.8V_{DDIO}	-	-	V
V_{IL}	Low level input voltage			-	-	0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY_N,	IOH = -100uA	0.8V_{DDIO}	-	-	V
V_{OL}	Low level output voltage		IOL = 100uA	-	-	0.2V_{DDIO}	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Islp_VDD	Sleep mode current	VDD	- DC/DC off - No clock - No output load - MCU interface access - RAM data access	-	20	TBD	uA
Idslp_VDD	deep sleep current	VDD	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data	-	1	TBD	uA
Iopr_VDD	Operating Mode current	VDD	VDD=3V After PON Command VGH=20V VGL=-VGH VSH=15V VSH2=15V VSL=-15V VCOM = -2V No waveform transitions. No output load No RAM read/write	-	2	-	mA
V_{GH}	Operating Mode Output Voltage	VGH		19.5	20	20.5	V
V_{SH}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		14.8	15	15.2	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

12 AC Characteristics

12.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, T_{OPR} = 25°C, CL=20pF

Table 12-1: Serial Peripheral Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	60			ns
t_{SCH}	CSB select hold time	65			ns
t_{SCC}	CSB deselect setup time	25			ns
t_{CHW}	CSB deselect hold time	100			ns
t_{SCYCW}	Serial clock cycle (Write)	50			ns
t_{SHW}	SCL “H” pulse width (Write)	25			ns
t_{SLW}	SCL “L” pulse width (Write)	25			ns
t_{SCYCL}	Serial clock cycle (Read)	400			ns
t_{SHR}	SCL “H” pulse width (Read)	180			ns
t_{SLR}	SCL “L” pulse width (Read)	180			ns
t_{SDS}	Data setup time	30			ns
t_{SDH}	Data hold time	30			ns
t_{DCS}	DC setup time	40			ns
t_{DCH}	DC hold time	40			ns
t_{ACC}	Access time			100	ns
t_{OH}	Output disable time	15			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

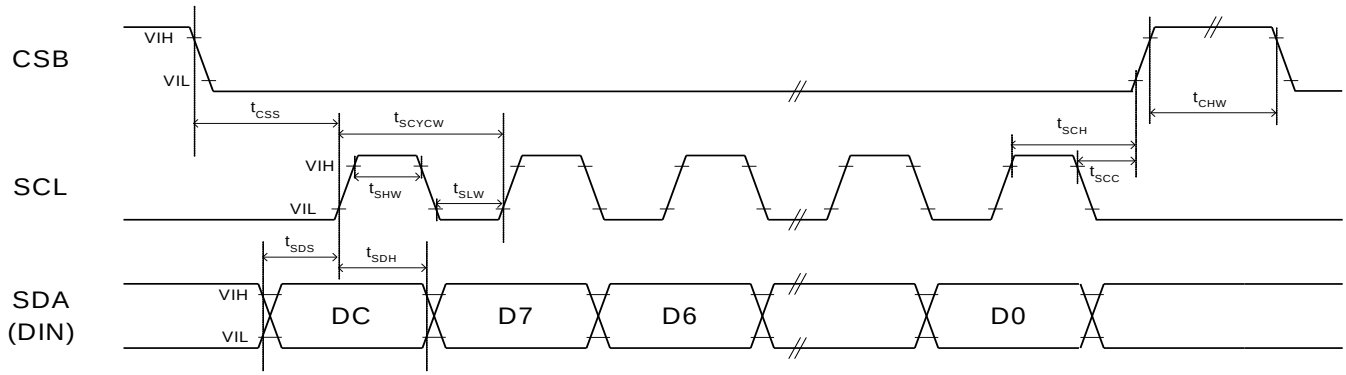


Figure 12-1: 3-wire SPI characteristics (write mode)

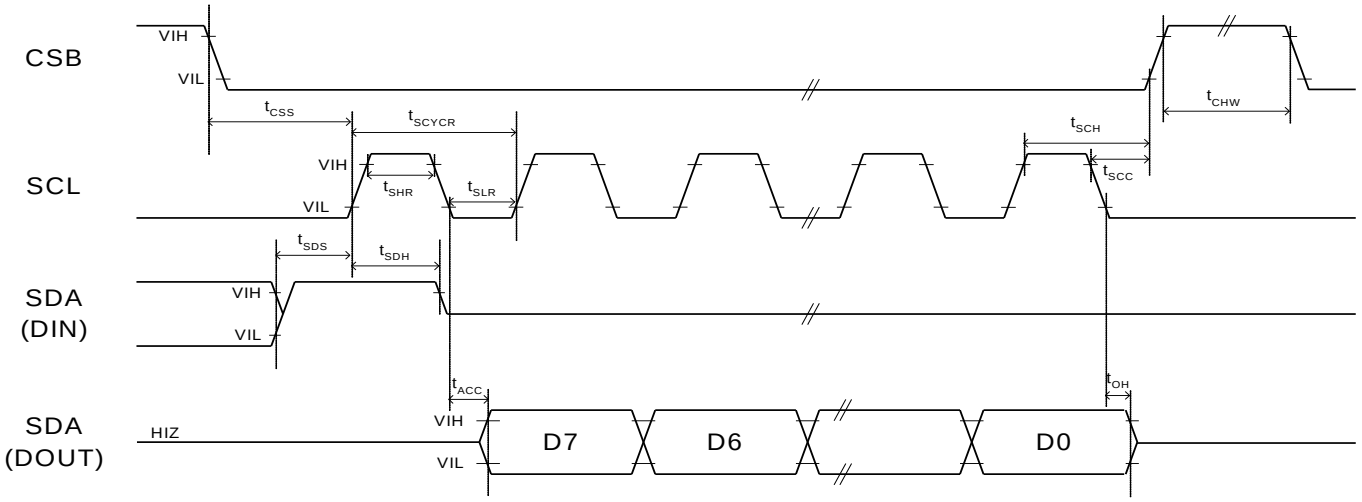


Figure 12-2: 3-wire SPI characteristics (read mode)

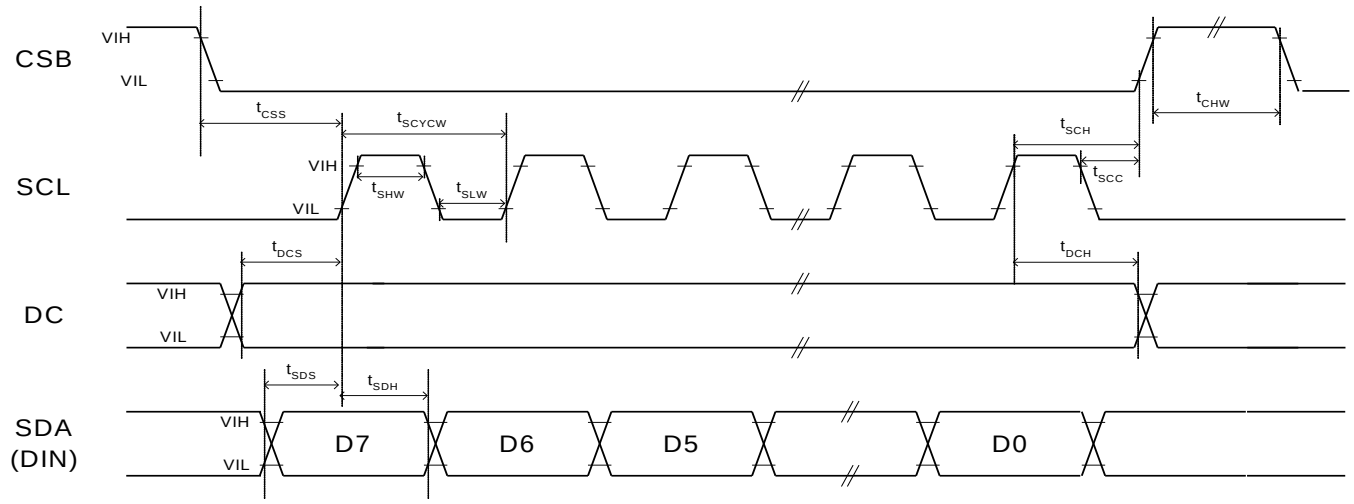


Figure 12-3: 4-wire SPI characteristics (write mode)

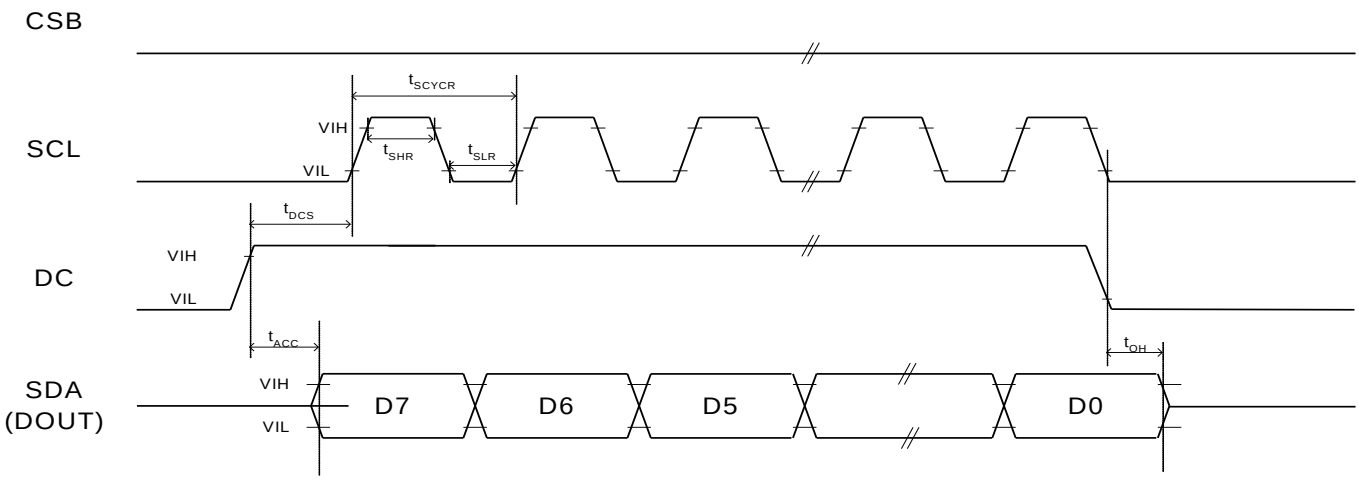


Figure 12-4: 4-wire SPI characteristics (read mode)

13 Application Circuit

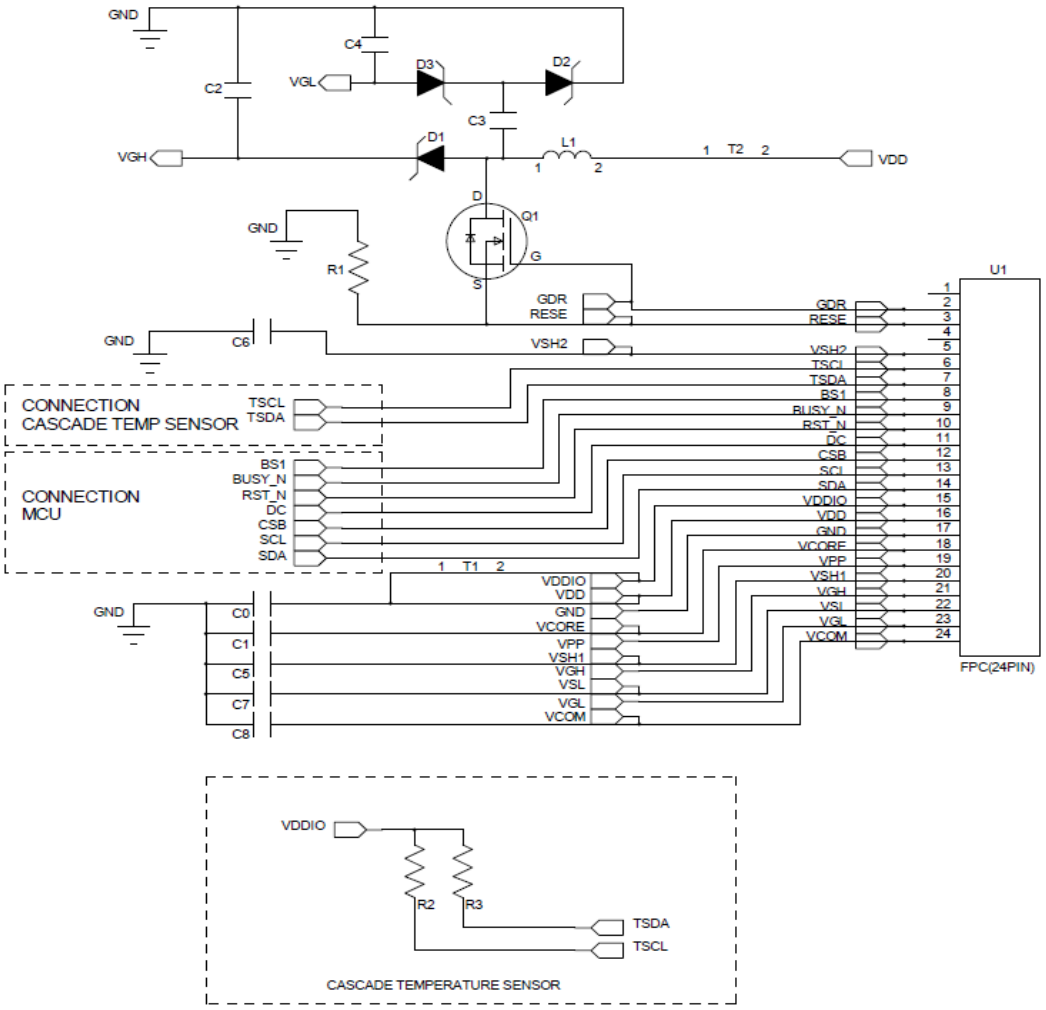


Figure 13-1: SSD2683 application circuit

Table 13-1: Component list for SSD2683 application circuit

Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≤ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

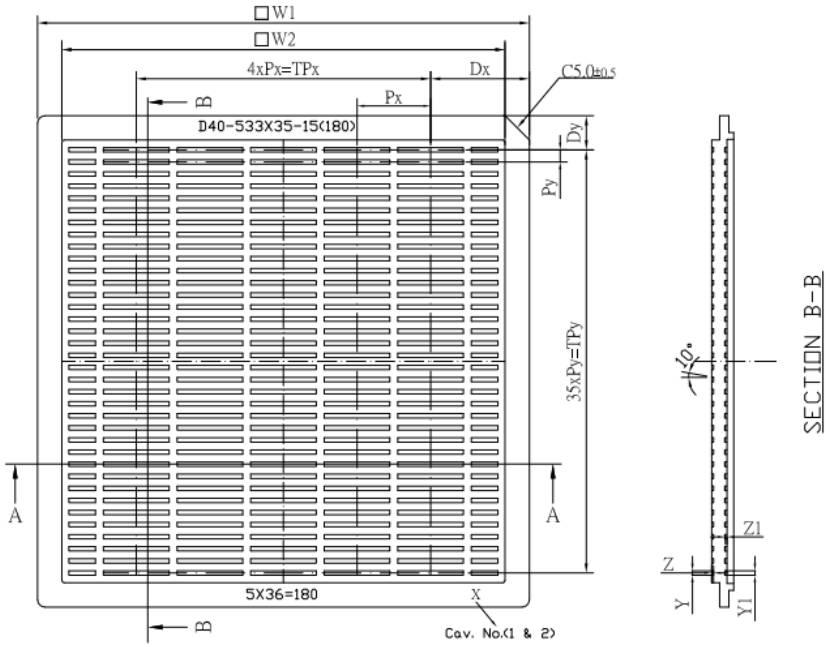
Remarks:

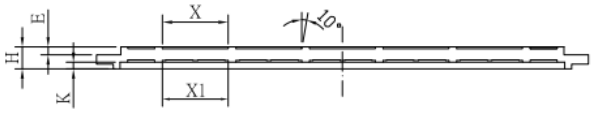
1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

14 Package Information

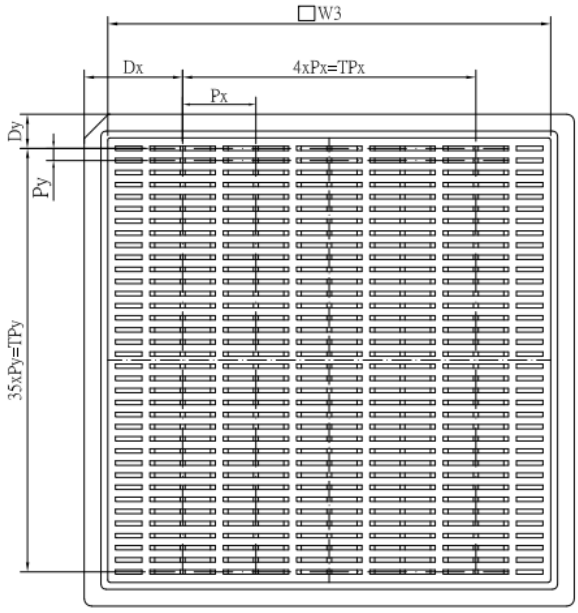
14.1 Die Tray Dimensions for SSD2683Z2 / SSD2683ZA

Figure 14-1: SSD2683Z2 / SSD2683ZA die tray information (unit: mm)





SECTION A-A



Symbol	Spec(mm)	(mil)
W1	101.60±0.10	(4000)
W2	91.55±0.10	(3604)
W3	91.85±0.10	(3616)
H	4.55±0.10	(179)
E	1.65±0.10	(65)
K	1.40±0.10	(55)
Px	15.20±0.05	(598)
Py	2.50±0.05	(98)
Dx	20.40±0.05	(803)
Dy	7.05±0.05	(278)
TPx	60.80±0.10	(2394)
TPy	87.50±0.10	(3445)
X	13.53±0.05	(533)
Y	0.89±0.05	(35)
Z	0.38±0.05	(15)
X1	13.53±0.05	(533)
Y1	0.89±0.05	(35)
Z1	0.35±0.05	(14)
N	5x36=180(Pocket Number)	

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